EUROPEAN TELECOMMUNICATION STANDARD

ETS 300 011

April 1992

Source: ETSI TC-TM

Reference: DE/TM-0310

ICS: 33.080, 33.040, 33.040.50

Key words: ISDN, primary rate user-network interface, testing

Integrated Services Digital Network (ISDN); Primary rate user-network interface Layer 1 specification and test principles

ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE
Office address: 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
X.400: c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

Contents

Blank page

Foreword

This European Telecommunication Standard (ETS) was produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS aims to meet urgent requirements of network operators and equipment manufacturers who are designing equipment to operate with an Integrated Services Digital Network (ISDN) primary rate access user-network interface. This ETS shall replace CEPT Recommendation T/L 03-14 (November 1987).

This ETS is based upon CCITT Recommendation I.431 (1988) [9] and provides modifications and further requirements to that base document. It also is affected by CCITT Recommendations G.703 [2], G.704 [3] and G.706 [4] (1988), and modifications and statements to these CCITT Recommendations are provided within this ETS.

This ETS also takes into account requirements contained in ECMA Standard 104: "Physical layer at the primary rate access interface between data processing equipment and private switching networks (1985)", which are given in Annex B.

Blank page

1 Scope

This European Telecommunication Standard (ETS) specifies requirements and test principles for the ISDN 72048 kbit/s primary rate user-network interface including the physical, electrical and functional characteristics and the information exchange with higher layers. Compliance with this ETS ensures that, with regard to layer 1 interface aspects, equipment for use with ISDN primary rate access is portable within countries that adhere to this ETS and, furthermore, that interworking with higher layer protocols for ISDN is supported.

This ETS is applicable to equipment having interface I_a or I_b for the connection to the ISDN primary rate user-network interface intended to be installed on customers' premises. In accordance with CCITT Recommendation I.411 [10], this ETS is to be applied to interfaces at reference points S, T and S/T (coincident S and T) of the ISDN reference configuration.

This ETS is applicable for ISDN channel arrangements as defined in CCITT Recommendation I.412 [11], as far as the primary rate at 2048 kbit/s is concerned.

This ETS is based on CCITT Recommendation I.431 [9] and gives further requirements or modifications to that Recommendation. Furthermore, this ETS identifies for each clause of CCITT Recommendation I.431 [9] whether it is regarded as normative, informative or as not relevant in the sense of an ETS.

This ETS also specifies, in Annex A, reference configurations and special requirements for application of this interface as a user-network interface for leased lines or as a user-user interface in particular for Private Telecommunications Network Exchange (PTNX) interconnections.

Annex B specifies additional requirements for interfaces at reference point S.

Annex C to this ETS specifies the relevant test principles to verify the requirements, and for testing conformance to this ETS. It is outside the scope of this ETS to define the static conformance requirements an equipment has to meet for attachment approval to a public network.

This ETS does not specify:

- safety requirements;
- interface or equipment overvoltage protection requirements;
- immunity requirements against electromagnetic interferences;
- emission limitation requirements.

2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references subsequent amendments to, or revisions of, any of these publications apply to this ETS only when incorporated in it by amendments or revision. For undated references the latest edition of the publication referred to applies.

[1] ETS 300 012 (1992): "Integrated Services Digital Network (ISDN); Basic rate user-network interface, Layer 1 specification and test principles".

[2] CCITT Recommendation G.703 (1988): "Physical/electrical characteristics of hierarchical digital interfaces".

[3] CCITT Recommendation G.704 (1988): "Synchronous frame structures used at primary and secondary hierarchical levels".

[4] CCITT Recommendation G.706 (1988): "Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704".

[5] CCITT Recommendation O.151 (1988): "Error performance measuring equipment for digital systems at the primary bit rate and above".

[6] ETS 300 125: "Integrated Services Digital Network (ISDN); User-network interface data link layer specification, Application of CCITT Recommendations Q.920/I.440 and Q.912/I.441".

[7] prEN 50096: "Integrated Services Digital Network (ISDN); Equipment with ISDN user-network interface at basic and primary rate, EMC requirements".

[8] Final draft prETS 300 046: "Integrated Services Digital Network (ISDN); Primary rate access - safety and protection".

[9] CCITT Recommendation I.431 (1988): "Primary rate user-network interface - Layer 1 specification".

[10] CCITT Recommendation I.411 (1988): "ISDN user-network interfaces - Reference configurations".

[11] CCITT Recommendation I.412 (1988): "ISDN user-network interfaces".

[12] ISO/IEC 10173: "Information Technology Integrated Services Digital Network (ISDN Primary Access Connector at Reference Point S and T)".

[13] ENV 41001 (1987): "ISDN Connector up to 8 pins and up to 2,048 M bit/s".

[14] ETR 001: "Integrated Services Digital Network (ISDN); Customer access maintenance".

[15] EN 60950 (1990): "Safety of information technology equipment including electrically operated business machines".

3 Definitions

For the purpose of this ETS the following definitions, together with those given in Clause 3 of ETS 300 012 [1] and in CCITT Recommendation I.411 [10] apply. Further definitions are given in Annex B.

Terminal equipment (TE): an equipment providing an interface I_a.

NOTE: This term is used in this ETS to indicate terminal-terminating aspects of TE1, TA and NT2 functional groups, where these have an I_a interface.

Terminal equipment type 1 (TE1): this functional group includes functions belonging to the functional group TE, and with an interface that complies with the ISDN user-network interface standard.

Network termination (NT): an equipment providing interface I_b

NOTE: This term is used in this ETS to indicate network-terminating aspects of NT1 and NT2 functional groups where these have an I_b interface.

Network termination type 1 (NT1): this functional group includes functions broadly equivalent to layer 1 (physical) of the OSI reference model. These functions are associated with the proper physical and electromagnetic termination of the network. NT1 functions are:

- Line transmission termination;
- layer 1 maintenance functions and performance monitoring;
- timing;
- layer 1 multiplexing;
- interface termination.

Network termination type 2 (NT2): this functional group includes functions broadly equivalent to layer 1 and higher layers of the CCITT Recommendation X.200 reference model. Private Automatic Branch Exchanges (PABXs), local area networks and terminal controllers are examples of equipment or combinations of equipment that provide NT2 functions. NT2 functions include:

- layer 2 and 3 protocol handling;
- layer 2 and 3 multiplexing;
- switching;
- concentration;
- maintenance functions;
- interface termination and other layer 1 functions.

Terminal adapter (TA): an equipment with interface I_a and one or more auxiliary interfaces that allow non-ISDN terminals to be served by an ISDN user-network interface.

Interface I_a: user side of the ISDN user-network interface for the primary rate access.

Interface I_b: network side of the ISDN user-network interface for the primary rate access.

4 Abbreviations

For the purpose of this standard the following abbreviations apply:

AIS	Alarm Indication Signal
CCITT	Consultative Committee on International Telegraphy and Telephony
CRC	Cyclic redundancy check
FC	Fault Condition
HDB3	High-Density Bi-polar 3 (line code)
ISPBX	Integrated Services Private Branch Exchange
IUT	Implementation Under Test
MPH	Management Primitives
NOF	Normal Operational Frames
NT	Network Termination
PABX	Private Automatic Branch Exchange
PH-AI	Primitive Active Indication
PH-DI	Primitive de-activate indication
PNT	Private Network Termination
PTN	Private Telecommunications Network
PRBS	Pseudo-Random Bit Sequence
PTNX	Private Telecommunications Network Exchange
RAI	Remote Alarm Indication
TA	Terminal Adaptor
TE	Terminal Equipment

Further abbreviations relevant to the test definitions are given in Annex C, Clause C.4.

5 Conformance

Conformance to this ETS can be claimed if the requirements contained in this ETS are complied with when tested according to the tests specified in Annex C.

The only exceptions are the following options:

- either CRC option 1 or CRC option 2 on the network side of the interface;
- the capability of the user side of the interface to support the application as user-network interface for leased line or user-user interface (Annex A);
- the application of the interface structures for different types of channels as defined in CCITT Recommendation I.412 [11];

- the use of bit 2 of timeslot O not containing the frame alignment signal, according to CCITT Recommendation G.706 [4], paragraph 4.

An equipment intended to be used at the S reference point shall conform to Annex B.

An interface at TE intended to be used as a user-network interface for leased lines or as a user-user interface shall meet the requirements of this ETS including those given in Annex A.

6 Requirements

The requirements to this ETS are given in CCITT Recommendation I.431 [9], together with the following statements, modifications and additional requirements to that Recommendation given in table 1 of this ETS.

References in CCITT Recommendation I.431 [9] to CCITT Recommendation I.604 should be read as to ETR 001 [14] (which is a delta document to CCITT Recommendation I.604) and those to CCITT Recommendation I.451 should be read as to ETS 300 102 Part 1.

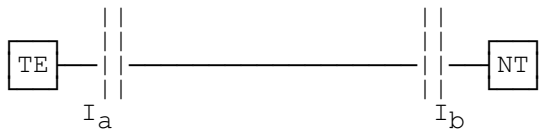
As CCITT Recommendations I.431 [9], G.703 [2], G.704 [3] and G.706 [4] are only recommendations, it is necessary to indicate the status of the Clauses for the purposes of this ETS, therefore tables 1 to 4, which refer to CCITT Recommendations I.431 [9], G.703 [2], G.704 [3] and G.706 [4] respectively, indicate the status of each Clause as defined below.

Definitions:

N	Normative: Requirements with which it is necessary to comply in order to be able to claim compliance with this ETS. Therefore, functions and features in Clauses of CCITT Recommendation I.431 [9], stated as being normative in this ETS, shall be implemented and followed even if the text is given as a recommendation or an example.
I	Informative: The text of this Clause is provided for information only. Titles for Clauses and subclauses are marked as informative when the requirements are given in further subclauses.
N/R	Not relevant: This Clause is not relevant to this ETS.

Notes under normative Clauses of these CCITT Recommendations are to be considered as informative unless otherwise stated in the relevant table to this ETS.

Table 1: Modifications and statements to CCITT Recommendation I.431 [9]

Clause/ subclause	Title/comment	Statement
1	Introduction	I
1.1	Scope and field of application	I
2	Type of configuration	I
2.1	Point-to-point	N
2.2	Location of interface	N
	<new text>	
	The electrical characteristics apply to the interface points I_a and I_b of figure 1	
		
	Figure 1: Location of interfaces	
	NOTE: I_a is located at the input and output ports of the TE. I_b is located at the input and output ports of the NT.	
3	Functional characteristics	I
3.1	Summary of functions (layer 1)	N
	<Replace the note to figure 2/I.431 with the following note>	
	NOTE: This power feeding function uses a separate pair of wires.	
3.2	Interchange circuits	N
	<Replace the last sentence of subclause 3.2 with the following>	
	The two wires of the pairs carrying the digital signal may be reversed	
3.3	Activation/deactivation	I
3.4	Operational functions	I
3.4.1	Definition of signals at the interface <The note to table 1/I.431 is not relevant.>	N
	<Add a new note to table 1/I.431>	
	Contiguous CRC blocks with errors shall result in contiguous CRC error information	
	<Add the following text at the end of subclause 3.4.1>	

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement

	The detection algorithm for signals given in table 1/I.431 and others is defined as follows:
	
	- Normal operational frames: the algorithm shall be in accordance with CCITT Recommendation G.706 paragraphs 4.1.2 and 4.2
	
	- Loss of frame alignment: the algorithm shall be in accordance with CCITT Recommendation G.706 paragraph 4.1.1.
	
	- RAI: RAI is detected when both of the two following conditions occur:
	
	  - frame alignment condition,
	
	  - reception of one bit A with binary content ONE.
	
	- Loss of signal: the equipment shall assume "loss of signal" when the incoming signal amplitude is more than 20 dB below the nominal output amplitude defined in CCITT Recommendation G.703 for this interface for more than 1 ms.
	
	  NOTE: The detection of this event is necessary if an implementation cannot detect loss of frame alignment in case of loss of incoming signal.
	
	- AIS: AIS is detected when both of the two following conditions occur:
	
	  - loss of frame alignment
	
	  - Reception of 512 bit periods containing less than 3 binary ZEROs (reference is made to CCITT Recommendation 0.162 paragraph 3.3.2)
	
	- CRC error information: reception of one E bit set to ZERO according to table 1/I.431.
	
	- RAI and continuous CRC error information: this event is identified when A bit set to ONE and E bit set to ZERO are continuously received within a persistence check time period of between 10 ms and 50 ms.	

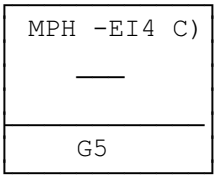
continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	- No signal: it is to be understood that the term "no signal" characterizes a range of transmitted signal levels which do not necessarily have a zero pulse amplitude but may be interpreted by a receiver as "loss of signal". - Loss of power or return of power: these are equipment internal events and do not require further definition of the detection mechanism.	
3.4.2	Definitions of state tables at network and user sides <Modify NOTE 1 to subclause 3.4.2 as follows> NOTE 1: Only those stable states needed for operation and maintenance of user and network side of the interface (system reactions, user and network responsible information) are defined. The transient states relative to the detection of CRC error information, AIS and RAI are not taken into account. It has to be taken into account that during state transitions error indication primitives PH and MPH are sent to higher layers. <Add the following text to end of subclause 3.4.2> The TE and NT shall inform layer 2 (of the D-channel protocol), the management entity and the other side of the interface of the status identified by the equipment according to the state tables.	N
3.4.3	Layer 1 states on the user side of the interface <NOTE 2 is not relevant.>	N
3.4.4	Layer 1 states at the network side of the interface <NOTE 2 is not relevant.>	N
3.4.5	Definition of primitive	N
3.4.6	State tables	N

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	<NOTE b) to table 2/I.431 is not relevant>	
	<Table 3/I.431, state G5, add in the third line: "signal transmitted toward the interface">	
	RAI, CRC error information	
	<Table 3/I.431, state G4, event FC4, the box shall read:>	
		
4	Interface at 1544 kbit/s	N/R
5	Interface at 2048 kbit/s	I
5.1	Electrical characteristics	N
	<New text>	
	This interface shall conform to CCITT Rec. G.703 paragraph 6, which specifies the basic electrical characteristics applying the balanced 120 ohm (symmetrical pair) cabling.	
5.2	Frame structure	I
5.2.1	Number of bits per timeslot	N
5.2.2	Number of timeslots per frame	N
5.2.3	Assignments of bits in timeslot 0	N
5.2.4	Timeslot assignment	I
5.2.4.1	Frame alignment signal	N
5.2.4.2	D-channel	N

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
5.2.4.3	B-channel and H-channels <Delete "NOTE 1" and add the text of NOTE 1 at the end of the second paragraph of subclause 5.2.4.3.>	N
5.2.4.4	Bit sequence independence	N
5.3	Timing considerations <Add the following sentences at the end of subclause 5.3> See also Annex A.3.1.1 Any TE which provides more than one interface is declared to be a multiple access TE and shall be capable of taking the synchronizing clock frequency for its internal clock generator from more than one access (or all access links) and synchronize the transmitted signals at each interface accordingly. A TE which is designed to be connected to the T reference point only, shall be able to synchronise at the nominal bit rate ± 5 ppm. A TE with free running clock frequency accuracy better than ± 1 ppm shall be able to synchronise at the nominal bit rate ± 1 ppm.	N
5.4	Jitter	I
5.4.1	General considerations	N
5.4.2	Minimum tolerance to jitter and wander at TE inputs <NOTE 2 is not relevant and replaced by the normative requirements given in Annex A>. <Add the following sentence to subclause 5.4.2> A TE with multiple accesses shall respect the worst case phase deviation between TE inputs of maximum 41 UI. <Replace NOTE 1 to fig.7/I.431 by the following:>	N

continued

Table 1 (continued)

<table>
<tr><th>Clause/ subclause</th><th>Title/comment</th><th>Statement</th></tr>
<tr><td></td><td>NOTE 1: Jitter/wander is Maximum Time Interval Error (MTIE) as defined in CCITT Rec. G.811 [16] and specified in CCITT Rec. G.823 [17], para. 2.2. In practice, this jitter/wander is superimposed upon a timing signal which is reasonably stable (c.f. CCITT Rec. O.171 [18]). In the worst case the phase deviation of a TE input from another TE input, in the multiple access configuration, can at maximum be twice the value A0 given in the table above.</td><td></td></tr>
<tr><td>5.4.3</td><td>TE and NT2 output jitter.</td><td>N</td></tr>
<tr><td>5.4.3.1</td><td>TE and NT2 with only one user-network interface.

<Replace the text of this subclause by the following one>.

The peak-to-peak output jitter shall meet the limits when measured with a bandpass filter having a high pass of first order (slope of 20 dB/decade) with cutoff frequencies as defined below. At the input the signal shall be provided with the tolerable input jitter specified in table 1, subclause 5.4.2, and with tolerable frequency deviation during measurement. Tests shall be made with Normal Operational Frames as well as AIS.

<table><tr><th colspan="2">Measurement filter bandwidth</th><th>Output jitter</th></tr><tr><th>Lower cutoff (high pass)</th><th>Upper cutoff (low pass)</th><th>UI peak-to-peak (maximum)</th></tr><tr><td>20 Hz</td><td>100 kHz</td><td>1,1 UI</td></tr><tr><td>400 Hz</td><td>100 kHz</td><td>0,11 UI</td></tr></table></td><td>N</td></tr>
<tr><td>5.4.3.2</td><td>TE and NT2 with more than one user-network interface to the same network

<Replace the text of this subclause by the following one></td><td>N</td></tr>
</table>

continued

Table 1 (continued)

<table>
<tr><th>Clause/ subclause</th><th>Title/comment</th><th>Statement</th></tr>
<tr><td></td><td>The peak-to-peak output jitter shall meet the limits when measured with a bandpass filter having a high pass of first order (slope of 20 dB/decade) with cutoff frequencies as defined below. At the input the signal shall be provided with the tolerable input jitter specified in table 1, subclause 5.4.2, and with tolerable frequency deviation during measurement. Tests shall be made with Normal Operational Frames.
<table>
<tr><th colspan="2">Measurement filter bandwidth</th><th>Output jitter</th></tr>
<tr><th>Lower cutoff (high pass)</th><th>Upper cutoff (low pass)</th><th>UI peak-to-peak (maximum)</th></tr>
<tr><td>4 Hz</td><td>100 kHz</td><td>1,1 UI</td></tr>
<tr><td>40 Hz</td><td>100 kHz</td><td>0,11 UI</td></tr>
</table>
Equipment with more than one interface using timing selection method (only one input, being in operational state, is used to synchronize the equipment clock at a point in time) may be considered as an equipment with one interface. In this case it shall meet the requirements of sub-clause 5.4.3.1 also during switch over to another interface (signal at input supplying timing changes from NOF with nominal frequency to AIS with plus or minus 50 ppm from the nominal frequency while all other inputs still receive NOF with the nominal frequency). The signals provided to the inputs shall carry tolerable jitter and may have deviation of bit-phase up to 0,5 UI.</td><td></td></tr>
<tr><td>5.5</td><td>Tolerable longitudinal voltage

<The reference in the note to figure 9/I.431 shall read>

see CCITT Recommendation O.9 [5]</td><td>N</td></tr>
<tr><td>5.6</td><td>Output signal balance

<This subclause is not any longer relevant. The requirement is now covered by prEN 50096 [7] (limitation of common mode voltages/currents).></td><td>N/R</td></tr>
</table>

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
5.7	Impedance towards ground	N
5.8	Interface procedures	I
5.8.1	Codes for idle channels and idle slots	N
5.8.2	Interframe (layer 2) time fill	N
5.8.3	Frame alignment and CRC-4 procedures	N
5.9	Maintenance at the interface	N
5.9.1	Definitions of maintenance signals	N
5.9.2	Use of CRC procedure	I
5.9.2.1	Introduction	N
5.9.2.2	Localization of the CRC functions in the subscriber access from the user point of view	I
5.9.2.2.1	No CRC processing in the transmission link	I
5.9.2.2.2	CRC processing in the digital transmission link	I
5.9.3	Maintenance functions	I
5.9.3.1	General requirements	N
5.9.3.2	Maintenance functions on the user side	I
5.9.3.2.1	Anomalies and defect detection	N
5.9.3.2.2	Detection of defect indication signals	N
5.9.3.2.3	Consequent actions	N
	<Delete the word "NOTE 1" so that the text is part of the main text.>	
	<Delete the NOTE 2 and add the following text to the subclause:>	
	The following points are required to ensure that an equipment is not removed from service or put into service due to short breaks in transmission or on detection of normal operational frames by layer 1 respectively.	

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	i) The persistent receipt of signals other than normal operational frames shall be verified by a timer T1 of 100 to 1000 ms before PH-DI is issued. ii) The persistent receipt of normal operational frames shall be verified by a timer T2 of 10 to 100 ms before PH-AI is issued. iii) T1 shall be suspended when T2 is started. T1 shall resume running when T2 is reset. iv) T1 shall be reset when T2 expires v) T2 shall be reset on receipt of signals other than normal operational frames.	
5.9.3.3	Maintenance functions on the network side	I
5.9.3.3.1	Defect detection	N
5.9.3.3.2	Detection of defect indication signals	N
5.9.3.3.3	Consequent actions	N
	<Delete the word "NOTE 1" so that the text is part of the main text.>	
	<Delete the NOTE 2 and add the following text to the subclause:>	
	The following points are required to ensure that an equipment is not removed from service or put into service due to short breaks in transmission or on detection of normal operational frames by layer 1 respectively.	
	i) The persistent receipt of signals other than normal operational frames shall be verified by a timer T1 of 100 to 1000 ms before PH-DI is issued.	

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	ii) The persistent receipt of normal operational frames shall be verified by a timer T2 of 10 to 100 ms before PH-AI is issued. iii) T1 shall be suspended when T2 is started. T1 shall resume running when T2 is reset. iv) T1 shall be reset when T2 expires v) T2 shall be reset on receipt of signals other than normal operational frames.	
6	Interface connector <New text> Interface connector and contact assignment are specified in ISO/IEC 10173 [12] and ENV 41001 [13]. However, permanent wiring connection of TEs to NTs is also permitted.	N
7	Interface wiring <New text> The magnitude of the characteristic impedance of "symmetrical type" interface cable shall be 120 ohm ± 20% in a frequency range from 200 kHz to 1 MHz and 120 ohm ± 10% at 1 MHz. The use of shielded interface cables may be required to meet radiation limitation and immunity requirements defined in the EMC standards (prEN 50096 [7]). Therefore the TE and the NT shall provide a point at the equipment where a shield of the interface cable can, and if provided shall be connected to. This point shall be designed respecting EMC requirements providing access to the signal reference for the transmitter and receiver of the equipment interface. Application of interface cable with individually shielded pairs or with a common shield for both pairs shall be possible.	N
8	Power feeding <New text>	N

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	The power feeding requirements of this standard are based on a single access NT1. A power source able to feed more than one NT1 (via a common pair of wires in the installation) shall meet the requirements at each individual power feeding interface at the same point in time. Customer access arrangements not using individual NT1 (e.g. higher order multiplexer system with multiplexed primary rate accesses) are outside the scope of this ETS and therefore subject for individual power feeding arrangements between customer and network provider.	
8.1	Provision of power <New text> The provision of power to the NT1 via the user network interface is mandatory. The power is provided by using a separate pair of wires to those used for transmission. Mandatory in this respect refers either to - the ability of the NT to be fed under the responsibility of the user when requested by the network provider. - the ability of the NT to be fed by a power supply unit under the responsibility of the network provider connected to the mains electric supply in the customer premises. In the case when the power is supplied by the user then the following two options are available to the user to provide the power supply - as an integral part of the TE, or - physically separated from the TE as an individual power supply unit.	N
8.2	Power available at the NT	N

continued

Table 1 (continued)

Clause/ subclause	Title/comment	Statement
	<New text> The power available at the input of the NT1 via the user-network interface when provided, shall be at least 7 watts	
8.3	Feeding voltage <New text> The feeding voltage at the input of the NT1 shall be in the range of -20 to -57 volts relative to ground.	N
8.4	Safety requirements <New text> In principle, safety requirements are outside the scope of this ETS. However, in order to harmonize power source and sink requirements the following is required: i) the power source shall be protected against short circuits and overload ii) The power sink of NT1 shall not be damaged by an interchange of wires With respect to the feeding interface of the power source, which is regarded as a touchable part in the sense of EN 60950 [19], the requirements are defined in ETS 300 046 [8].	N
Annex A	Timeslot assignment for interfaces having only Ho-channels <Delete subparagraph A.1>	I
Annex B	Timeslot assignment for 2048 kbit/s interfaces having H11-channels <Replace the existing table with the following:>	I

continued

Table 1 (concluded)

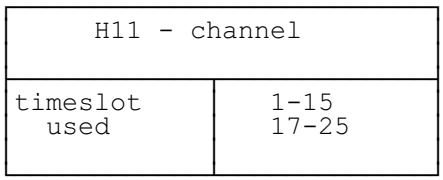
Clause/ subclause	Title/comment	Statement
		
Appendix I	Pulse mask for interface at 1544 kbit/s	N/R

Table 2: Modifications and statements to CCITT Recommendation G.703 [2]

Clause/ subclause	Title/comment	Statement
1 to 5		N/R
6	Interface at 2048 kbit/s	I
6.1	General characteristics	N
6.2	Specifications at the output ports	N
	<Delete column "one coaxial pair", the interface for the symmetrical pair shall be applied.>	
	<"Maximum peak-to-peak jitter at the output port" is not relevant, see table 1, 5.4.3>	
6.3	Specification at the input ports	N/R
6.3.1		N
6.3.2	<See table 1, 5.4.2>	N/R
6.3.3		N
6.3.4		N
6.4	Earthing of the outer conductor of screen	N/R
	<See prETS 300 046 [8] and table 1, Clause 7>	
7 to 11		N/R
Annex A	Definition of codes	N
	<HDB3 code only>	
Annex B	Specification of the overvoltage	N/R
	<Covered by prETS 300 046 [8]>	

Table 3: Modifications and statements to CCITT Recommendation G.704 [3]

Clause/ subclause	Title/comment	Statement
1	General	N/R
2	Basic frame structures	I
2.1, 2.2		N/R
2.3	Basic frame structure at 2048 kbit/s	I
2.3.1	Frame length	N/R
	<See table 1, 5.2>	
2.3.2	Allocation of bits numbers 1 to 8 of the frame	N
	NOTE 1	N/R
	<See table 3, 2.3.3 and table 1, 5.2.3 and 5.9.2.1>	
	NOTE 4	N/R
	<See table 1, 5.2.3>	
2.3.3	Description of the CRC4 procedure in bit 1 of the frame	N
	<NOTE 1 in 2.3.3.4 is normative>	
2.4		N/R
3 and 4		N/R
5	Characteristics of frame structure carrying channels at various bit rates in 2048 kbit/s interface	N/R
	<See table 1, 5.2.4>	
6		N/R
Annex	Examples of CRC implementations using shift registers	I

Table 4: Modifications and statements to CCITT Recommendation G.706 [4]

Clause/ subclause	Title/comment	Statement
1 to 3		N/R
4	Frame alignment and CRC procedure at 2048 kbit/s interface	I
4.1	Loss and recovery of frame alignment	I
4.1.1	Loss of frame alignment	N
4.1.2	Strategy for frame alignment recovery	N
	NOTE	N
4.2	CRC multiframe alignment using information in bit 1 of the basic frame	N
	NOTE 1	N
	NOTE 2	N
4.3	CRC bit monitoring	N
4.3.1	Monitoring procedure	N
4.3.2	Monitoring for false frame alignment	N
	NOTE 1	N
	NOTE 2	N
4.3.3	Error performance monitoring using CRC4	I
	<This function is optional, see also table 1, 5.9.3.2.2 and 5.9.3.3.3>	
5		N/R
Annex A	Background information on the use of CRC procedures	I

Annex A (normative): Application of the ETS 300 011 for PTNX interconnections (leased lines)

A.1 Introduction

According to the definitions of this ETS some of the functions crossing the interface are not symmetrical (e.g. timing, operation and maintenance, power feeding). For instance, the network side acts regarding the timing as a master, providing the network synchronous clock, while the user side in all cases acts as a slave, being synchronised to the network and looping back the timing received.

For leased line applications the master/slave relationship between the two PTNXs or between the PTNXs and the networks providing the leased line has to be re-defined. With two PTNXs immediately interconnected one of them shall be allocated the master function whereas the other one shall be allocated the slave function. With two PTNXs interconnected through an intervening network, the intervening network may be allocated the master function. However, the master function need not be the same as specified for the ISDN user-network interface in the main part of this ETS.

The definition for the case, where the same physical interface is to be used for inter-PTNX interconnections not involving a public ISDN, are contained in this Annex.

Conformance to this Annex requires fulfilment of subclauses A.3.1.1 and A.3.3.

NOTE: The application of permanent inter-PTNX connections via the ISDN (e.g. semipermanent connection using ISDN switching capabilities) are not part of the definitions and models given below. Such applications are generally covered by the user network interface specification given in the main part of this ETS.

A.2 Layer 1 modes of operation and interface/application models

Two modes of operation may be envisaged, point-to-point and point-to-multipoint.

In the point-to-point mode the interconnection of two PTNXs employs one interface at either PTNX. No segregation of information channels takes place in the network.

In the point-to-multipoint mode multiple interconnections with more than two PTNXs share the same interface, at least at one PTNX, and the information channels carried in the 2048 kbit/s stream is to be segregated by the network.

For the two modes of operation the application of both

- existing types of transmission equipment; and

- ISDN primary rate access in accordance with this ETS

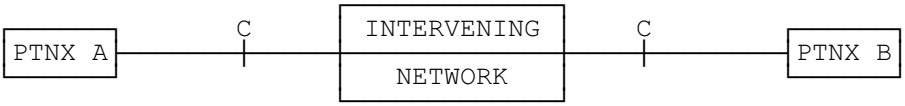
conveying the digital signal are considered.

NOTE 1: For clarity the models below show single interface applications at the PTNXs only. However, this does not imply any restriction from employing multiple access applications in private networks (unique or mixed type of models or modes of operation).

NOTE 2: Any impact of the possible use of inter-PTNX connections not adhering to the access associated signalling principle throughout the intervening network (as employed in ISDN user-network interface) is outside the scope of this ETS.

A.2.1 Point-to-point mode of operation

Functional model:



C = reference point for PTNX interconnection links.

NOTE: The intervening network may only be a wiring (see figure A.2).

Figure A.1: PTNX interconnection functional model in point-to-point mode of operation

Interface/application model:

KD = Interface at C reference point.

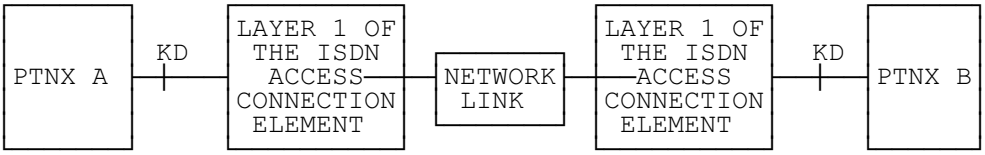
NOTE: Full transparent 2048 kbit/s stream between PTNXs.

Figure A.2: PTNX interconnection according to figure A.1 using interface transmission medium only

NOTE 1: Even in a single, fully transparent 2048 kbit/s stream between PTNXs the digital section/link may intervene in specific cases (e.g. insertion of AIS).

NOTE 2: A digital link comprises one or more digital sections and may include multiplexer but not switching or cross connect systems.

Figure A.3: PTNX interconnection according to figure A.1 using digital section or digital link



NOTE: Layer 1 of ISDN access connection elements consist of the NT1 and LT as used in ISDN accesses and a functional block which performs some ET layer 1 functions. This functional block terminates and generates timeslot 0 functions including CRC4 and provides the clock for the access. At its link side it terminates and generates timeslot 0 functions of the link. Timeslots 1 to 31 are transparent.

Figure A.4: PTNX interconnection according to figure A.1 using two ISDN access connection elements

If CRC4 option 1 is used (see ETR 001 [14]), timeslot 0 and CRC4 are terminated in ET layer 1 and PTNX.

If CRC4 option 2 is used timeslot 0 is terminated in ET layer 1 and PTNX but CRC4 is terminated in ET layer 1, NT1 and PTNX.

A.2.2 Multipoint mode of operation

Functional model:

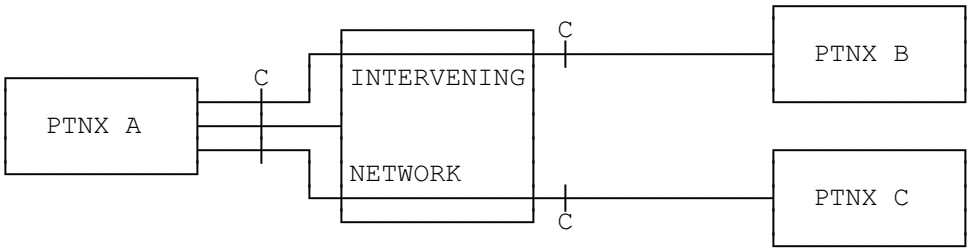


Figure A.5: PTNX interconnection functional model in point to multipoint mode of operation

Interface/application model:

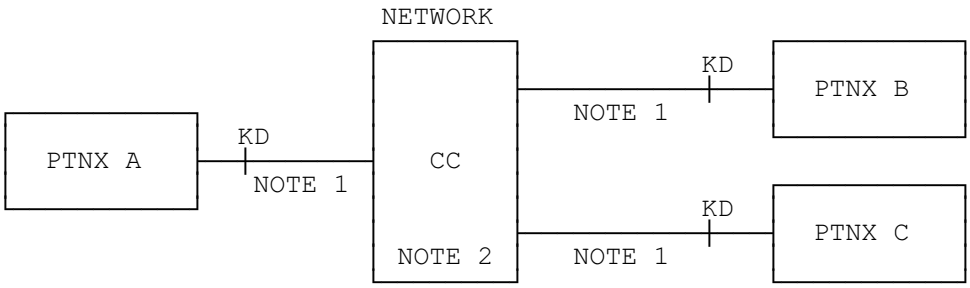


Figure A.6: PTNX interconnection according to figure A.5 using different types of techniques to connect to the cross connect function

NOTE 1: The three alternative models given in figures A.2 to A.4 above may be applied to connect the PTNX to the CC (Cross Connect). These combined models are called hereafter A.6/2, A.6/3 and A.6/4 respectively.

NOTE 2: CC stands for a configuration of a number of digital multiplex equipment and a distribution frame or a cross connect system. Timeslot 0 is terminated in the CC; only timeslots 1 to 31 are transparent between the PTNXs.

A.3 Special requirements

A.3.1 Timing requirements

A.3.1.1 Point-to-point mode of operation

The timing distribution figures in this subclause only show principles and do not necessarily relate to real implementation in equipment; other configurations may be used provided that the same functionality and capability is achieved.

If models according to figures A.2 and A.3 are applied a master/slave relationship shall be established between the two PTNXs.

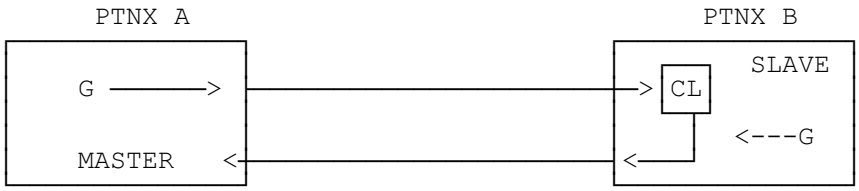


Figure A.7: Timing configuration of two PTNXs applying figures A.2 or A.3

G: Clock signal generator.

CL: Clock recovery function (e.g. clock input selection or averaging in case of more than one input).

A master/master configuration is also applicable if both PTNXs are synchronized by the same clock source independently (e.g. by the network).

The generator in PTNXs acting as a slave is used in case of loss of incoming clock to generate the output frame in this condition.

In a configuration consisting of more than 2 PTNXs connected together two clock distribution alternatives exist:

- PTNX A acts as a master for all interconnections (star master/slave configuration as in figure A.7);

- a clock distribution cascade may be applied (see figure A.8).

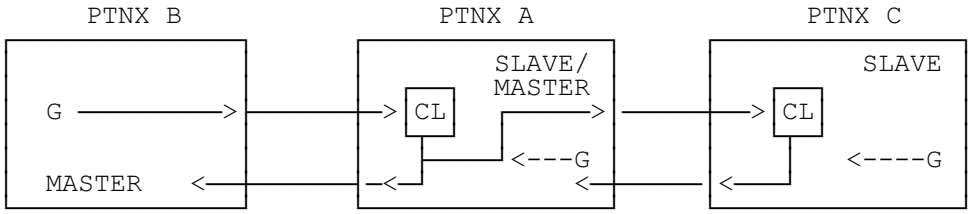


Figure A.8: Timing configuration of three PTNXs applying figures A.2 or A.3

If the model given in figure A.4 is applied then the ET layer 1 function in the access connection elements always act as the master and provide the clock to the PTNX (see figure A.9).

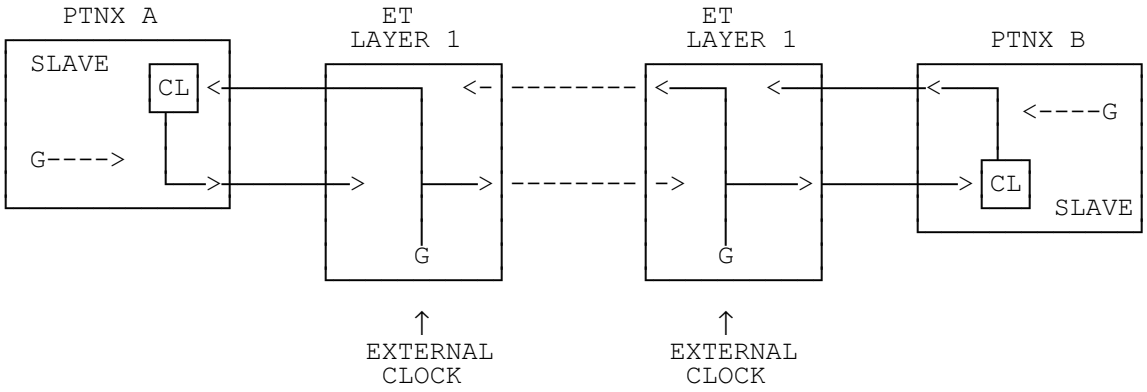


Figure A.9: Timing configuration of two PTNXs applying figure A.4

The clock shall always be provided by the PTNX interconnection link. However, the detailed configuration may vary in different implementations (e.g. the external clock may be provided to one ET layer 1 only and a clock loop back may be applied in the other ET layer 1).

A PTNX designed to act as a master when being in free running mode shall have an accuracy of the output frequency of ± 32 ppm.

A PTNX with a high clock accuracy class of better than ± 1 ppm may not be able to synchronise its internal clock to an input frequency with a tolerance of ± 32 ppm. The timing negotiation function being specified for private networks shall guarantee that the PTNX with the higher clock accuracy shall act as the master after re-establishment of the configuration.

A.3.1.2 Multipoint mode of operation

In this mode of operation the CC shall work in synchronised operation condition to guarantee slip performance limits. This requires that the CC acts as the master clock source if models A.6/2 and A.6/3 are applied and all PTNXs act as slaves. If model A.6/4 is applied the ET layer 1 function in the access connection elements act as the master (synchronised like the CC by the network's synchronisation concept) and the PTNX as slaves.

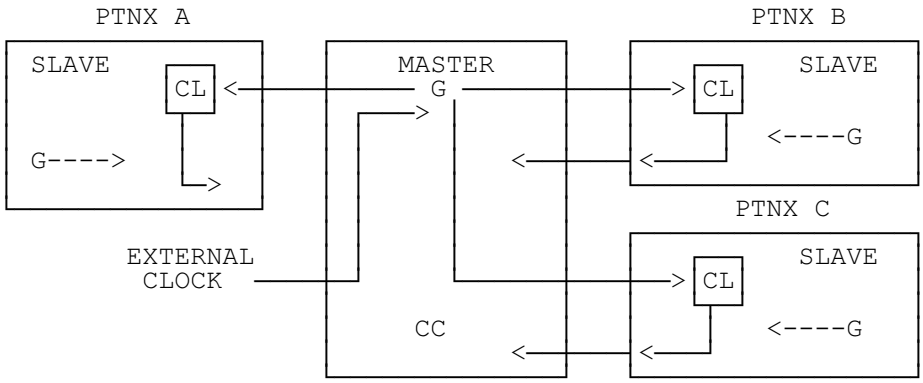


Figure A.10: Timing configuration of PTNXs applying figure A.6

A.3.2 Tolerable jitter and wander at inputs

The requirements given in table 1, subclause 5.4.2, shall be applied but the values given in table A.1 shall be applied.

Table A 1: Minimum tolerable jitter and wander at TE/NT2 for interfaces designed for PTNX interconnections

AO	A1	A3	f0	f1	f2	f3	f4
20,5 UI	1,5 UI	0,2 UI	12E-6 Hz	20 Hz	2,4 kHz	18 kHz	100 kHz

A.3.3 Output jitter

For a PTNX acting as a master (e.g. PTNX A in figure A.7) the output jitter shall be in accordance with the limits given in table 1, subclause 5.4.3.1.

The output jitter shall be in accordance with the requirements given in table 1, subclause 5.4.3.2 with tolerable input jitter as specified in subclause A.3.2 during measurement, but the values given in table A.2 shall be applied.

Table A.2: Output jitter limits

Measurement filter bandwith		Output jitter
Lower cut-off (high pass)	Upper cut-off (low pass)	Peak to peak (maximum)
4 Hz	100 kHz	1,6 UI
40 Hz	100 kHz	0,11 UI

A.4 Operation and maintenance

A PTNX may use an interface which follows the operational aspects defined in the F-state table (table 2/I.431 [9]) or even may use an interface according to this ETS for PTNX interconnections. At these interfaces the PTNX receives signals from the opposite side to indicate the state of the connection expressed to the PTNX management function in the form of management primitives (MPH). These primitives need to be interpreted by the management function dependent on the model applied for this interconnection (as given in Clause A.2).

The application of the operational functions and the F-state matrix of this ETS, implemented in a PTNX interface used for PTNX interconnections, is generally possible. However, some model dependent adaptations are required in the PTNX management function.

This concerns:

- the applicability of a function; and

- the control area of a function.

This information is given in table A.3.

The PTNX recognizes, for example, a specific signal (defined in table 1/I.431 [9]) at the input of its interface and is then forced to go to an F-state thereby issuing an error indication (MPH-EIn) to the management function in the PTNX according to table 2/I.431 [9]. However the fault conditions (FC1 to FC4) need to be re-allocated to the F-states. This can be done by a re-interpretation of the error indication primitives (MPH-EIn) by the PTNX management function which is given in table A.4.

This re-interpretation also takes into account the responsibility for a fault indicated by an error indication. Fault conditions FC2 and FC4, which correspond to the MPH-EI2 and 4 respectively, generally fall under the responsibility of the PTNX. With regard to MPH-EI1 and 3 they indicate a fault in the interconnection link.

Table A.3: Control area and applicability of the operational functions in point to point configuration and multipoint configuration via CC

Function/cause	Control area/consequence ISDN access interface	Model A.2	Model A.3	Model A.4	Models A.6/2 and /3	Model A.6/4
A CRC4						
A1 CRC4 PTNX maintenance entity	option 1: PTNX -ET option 2: PTNX -NT1	PTNX -PTNX	PTNX -PTNX	option 1: PTNX -ET layer 1 option 2: PTNX -NT1	PTNX -CC	option 1: PTNX -ET layer 1 option 2: PTNX -NT1
A2 CRC4 PTNX adjacent network maintenance entity	option 1: ET-PTNX option 2: ET-NT1	not applicable	not applicable	option 1: ET layer 1-PTNX option 2: ET layer 1-NT1	CC-PTNX	option 1: ET layer 1-PTNX option 2: ET layer 1-NT1
B Loss of frame alignment detected by PTNX	NT1-PTNX /PTNX is to send RAI (bit A = 1), PH-DI (loss of layer 1 capability)	PTNX -PTNX	PTNX -PTNX	option 1: ET layer 1-PTNX option 2: NT1-PTNX	CC-PTNX	option 1: ET layer 1-PTNX option 2: NT1-PTNX
C Reception of AIS by PTNX	ET-NT1/PTNX is to send RAI (bit A = 1), PH-DI (loss of layer 1 capability and network clock)	not applicable	applicable; Note 1	applicable	applicable	applicable
D Loss of incoming signal	NT1-PTNX /as for C	PTNX -PTNX Note 1	link-PTNX Note 1	NT1-PTNX	A.6/2 CC-PTNX A.6/3 link-PTNX	NT1-PTNX
E Reception of RAI (bit A=1)	PTNX -ET/PH-DI (loss of layer 1 capability)	PTNX -PTNX	PTNX -PTNX	ET layer 1-PTNX	CC-PTNX	ET layer 1-PTNX
F Reception of operational frames	PTNX -ET/PH-AI	PTNX -PTNX	PTNX -PTNX	PTNX -ET layer 1	PTNX -CC	PTNX -ET layer 1
G Sa bits received by PTNX	Not yet defined / Bit in position 1 and 8: ignore for the time being; bit in position 5 to 7: ignore	Sa bits may be used by PTNX		not defined / Bit in position 1 and 8: ignore for the time being; bit in position 5 to 7: ignore		
H Sa bits transmitted by PTNX	Not yet defined / Bit in position 1 and 8: not applicable for the time being: bit in position 5 to 7: not applicable	Sa bits may be used by PTNX s		not defined / Bit in position 1 and 8: not applicable for the time being, bit in position 5 to 7: not applicable		

NOTES to table A.3:

NOTE 1: The consequence "loss of network clock" is applicable for the slave side only.

NOTE 2: The terms option 1 and option 2 indicate the application of CRC4 int the digital transmission link as defined in CCITT Recommendation I.431 [9] paragraph 5.9.2.2:
- Without CRC4 processing in the transmission link = option 1;
- with CRC4 processing in the transmission link = option 2.

Table A.4: Re-interpretation of MPH-error indications in the ISPBX management entity

table 2/I.431 [9]					
MPH	state entered	A.2	A.3	A.6/2, A.6/3 A.4, A.6/4	A.4 option 2; A.6/4 option 2
EI0	F0	EI0	EI0	EI0	EI0
EI1	F2	EI4	EI1 and EI4 NOTE 2	EI1 and EI4 NOTE 2	EI1
EI2	F3	EI2	EI2	EI2	EI2
EI3	F4	-	EI3	EI3	EI3
EI4	F5	-	-	-	EI4
AI	F1	AI	AI	AI NOTE 1	AI NOTE 1

- = not applicable or not possible.

NOTE 1: The recovery from a fault condition discovered by an ISPBX is of local significance only. The exact control area indicated by this primitive can be taken from table A.3 (function F).

NOTE 2: No mechanism available to distinguish between the two failure conditions.

Annex B (normative): Application of ETS 300 011 to the S reference point

B.1 Scope

The scope of this Annex is the application of this ETS to the primary rate access interface at an S reference point, as provided by a Private Telecommunication Network Exchange (PTNX) to its terminals, see figure B.1.

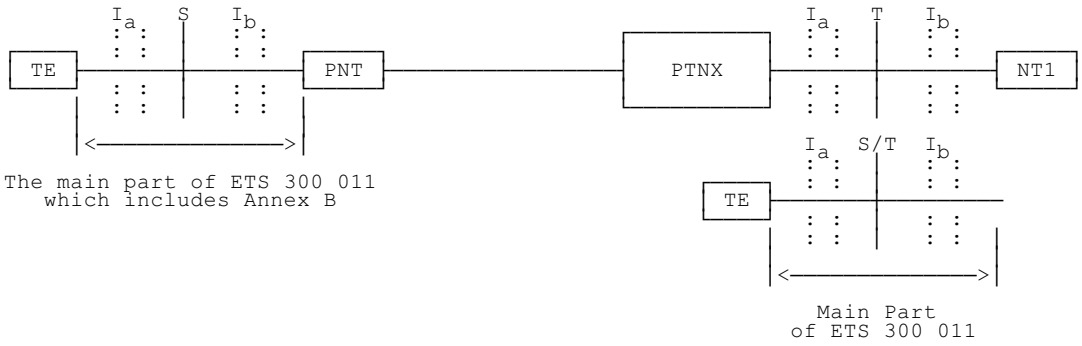


Figure B.1: Application of this ETS at various reference points

S, S/T, T = Reference points.

NOTE: The PNT (Private Network Termination) may be a separate equipment or incorporated in the PTNX.

B.2 Definitions

For the purpose of this Annex the following definitions apply, in addition to, or instead of, the definitions given in Clause 3 of the main part of this ETS.

S Interface: the interface according to the primary rate access structure as appearing at the S reference point of a Private Telecommunication Network Exchange.

Terminal Equipment: the definition in Clause 3 of the main part of this ETS applies with the exception that the NT2 functional grouping is not covered by this term within the context of this Annex.

Network termination: equipment providing interface I_b.

NOTE: In this Annex, this term is used to designate the network terminating functions of a PNT or of a PTNX, whatever provides interface I_b to the TE.

Private Telecommunication Network Exchange (PTNX): a nodal identity in a private telecommunication network which provides autonomous and automatic switching and call handling functions used for the provision of telecommunication services which are based on the definitions for those of the public ISDN.

Private Network Termination (PTN): a remote unit of equipment which terminates a transmission system employed between the PTNX and the interface I_b and the S reference point.

B.3 Conformance

Conformance to this Annex implies that the mandatory requirements of Clause 5 of the main part of this ETS are met, with the exception that the CRC4 procedure (table 4, Clause 4) is optional for equipment before January 1993, see also subclause B.4.3.

In addition, the following subclauses of this Annex shall be conformed to:

B.4.1, B.4.2, B.5, B.6.

B.4 Requirements

B.4.1 Timing considerations

In a condition where the PTN is not synchronized by a high precision master clock (e.g. of the public ISDN), the frequency deviation of its free running clock shall not exceed ± 32 ppm.

B.4.2 Jitter, general considerations

The PTN shall comply with the jitter characteristics as specified in subclause 5.4.2 of table 1. A PTN deriving its timing from the public ISDN shall meet the jitter characteristics specified for a TE with multiple accesses, see subclause 5.4.3.2 of table 1.

B.4.3 Frame alignment and CRC4 procedures

Operation without CRC4 procedure can be required, and shall be restricted, to cover interworking situations. S interfaces following this ETS, but, in addition, designed for interworking with equipment not supporting CRC4 procedures, shall provide a CRC-DISABLE management function which allows disabling of the CRC4 procedure.

When the CRC-DISABLE function is activated, the CRC multiframe alignment procedure shall be inhibited and the CRC error reporting function shall be fixed in a way that the CRC error report primitive "Local CRC-E1" would always indicate to the management entity that no CRC error had occurred.

When the CRC-DISABLE function is activated, Bit 1 of timeslot 0 shall always be set to ONE.

B.5 Interface wiring

The TE can be connected to the PTN either by permanent wiring or via connectors (see table 1, Clause 6). The connection cords shall be considered part of the wiring (see subclause C.1.3); they shall consist of two twisted and commonly or separately shielded pairs.

B.6 Loopbacks required at S reference point

Loopback 4, as defined in Annex D, shall be implemented.

It is to be noted that there is currently no protocol defined in the D-channel protocol to control loopback 4 remotely by a PTNX. In addition, to control loopback 4 from a remote point (e.g. a remote maintenance server or a remote user), a protocol mechanism is to be specified as applicable between the remote point and the TE or the remote point and the relevant PTNX.

Annex C (normative): Conformance test principles for the user and the network side of the interface

C.1 Scope and general information

C.1.1 Scope

This Annex provides the test principles for the requirements of this ETS used to determine the compliance of an implementation under test to this ETS.

It is outside the scope of this Annex to identify the specific tests required by an implementation where equipment has to meet attachment approval.

Detailed test equipment accuracy and the specification tolerance of the test devices is not a subject of this Annex. Where such details are provided then those test details are considered as being an "informative" addition to the test description.

The test configurations given do not imply a specific realisation of test equipment, or arrangement, or the use of specific test devices for conformance testing. However, any test configuration used shall provide those test conditions specified under "system state", "stimulus" and "monitor" for each individual test.

C.1.2 General information

This document is applicable to interfaces I_a and I_b as appropriate. The field of applicability is reported at the beginning of each test.

In the case of a multi-access implementation under test supporting interface I_a, unless otherwise stated, only one access at a time shall receive the stimulus. All other accesses shall receive "no signal" (state F3).

C.1.2.1 Additional information to support the test

It is assumed that, at least one of the following facilities is provided by IUT

1) a transparent loopback of at least one timeslot towards the interface;

2) the ability to transmit a PRBS 2^{11}-1 in a timeslot.

When the IUT does not provide these facilities the equipment supplier may provide:

a) a test equipment using the same chip set and interface components as in the IUT and able to provide a transparent loopback of at least one timeslot towards the interface; or

b) a test equipment using the same chip set and interface components as in the IUT and able to provide a PRBS 2^{11}-1 in a timeslot.

C.1.2.2 Definitions and abbreviations

For the purpose of this Annex the following definitions and abbreviations, together with those given in Clause 3 apply.

IUT (Implementation Under Test)

Implementation of interface related functions for:

- the user side of the interface (Ia), i.e. TE1, TA, NT2; and
- the network side of the interface (Ib), i.e. NT2, access connection element.

Rx Interface signal receiver of IUT or simulator.

Tx Interface signal transmitter of IUT or simulator.

Simulator - (terminal, network): device generating a stimulus signal conforming to this ETS to bring the IUT into the required operational state and monitoring the receive signal from the IUT. It can either be a simulator for the user side or the network side of the interface.

C.1.3 Connection of the simulator to the IUT

For testing the electrical characteristics of the IUT the simulator, or its relevant part, shall be connected directly to the interconnecting points for the interface wiring at the IUT unless otherwise stated. For the tests given in subclauses C.2.3, C.2.4, C.2.9, C.2.11 and Clause C.5, a cord connected at an IUT shall be removed since a cord is regarded as integral part of the interface wiring.

All other tests may be performed with interface wiring complying with the requirements given in table 1, Clause 7 and table 2, subclause 6.3.

C.1.4 Allocation of tests

The following tables allocate the requirements defined in table 1 of this ETS to the tests specified in this Annex.

Requirements of tables 2, 3 and 4 are covered as follows:

- table 2 is covered by table 1, subclause 5.1;
- table 3 is covered by table 1, subclauses 5.2 and 5.8.3;
- table 4 is covered by table 1, subclause 5.8.3.

One test definition may cover more than one requirement for one or both interface points (interface I_a or I_b). Requirements which do not need specific test definition are indicated by "not relevant" (N/R).

C.1.4.1 General

Functions	Clause/ Subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Introduction	1	N/R	
Scope and field of application	1.1	N/R	

C.1.4.2 Type of configuration requirements

Functions	Clause/ Subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Type of configuration	2	N/R	
Point-to-point	2.1	N/R	
Location of interface	2.2	I_a and I_b	see C.1.3

C.1.4.3 Functional characteristics requirements

Table, subclause C.1.4.3

Functions	Clause/ Subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Summary of functions (layer 1)	3.1		
B-channel		I_a and I_b	C.2.6
H0-channel		I_a and I_b	C.2.6
H1-channel		I_a and I_b	C.2.6
D-channel		I_a and I_b	C.2.6
Bit timing		I_a and I_b	C.2.7
Octet timing		I_a and I_b	C.2.5
Frame alignment		I_a and I_b	C.4.3
Power feeding		I_a and I_b	C.5
Maintenance		I_a and I_b	C.3.2
CRC procedures		I_a and I_b	C.4.3, C.4.4 and C.4.5
Interchange circuits	3.2		
Interchange circuits		N/R	
Power feeding interch.circuit		N/R	
Wire reversal		I_a and I_b	C.2.4.2
Activation/ deactivation	3.3	N/R	
Operational functions	3.4	N/R	
Definition of signals at the interface	3.4.1		
Normal Operational Frame		I_a and I_b	C.3.1.1
RAI		I_a and I_b	C.3.1.2
LOS		I_a and I_b	C.3.2
AIS		I_a I_b	C.2.7.1,C.3.2.2 C.3.1.3
CRC error information		I_a and I_b	C.3.1.4
Definitions of state tables at network and user sides	3.4.2	I_a and I_b	C.3.2

continued

Table, subclause C.1.4.3 (concluded)

Layer 1 states on the user side of the interface	3.4.3	I_a	C.3.2.2
Layer 1 states a the network side of the interface	3.4.4	I_b	C.3.2.1
Definition of primitive	3.4.5	N/R	
State tables	3.4.6		
F state table	2	I_a	C.3.2.2
G state table	3	I_b	C.3.2.1

C.1.4.4 Interface at 1544 Kbit/s requirements

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Interface at 1544 kbit/s	4	N/R	

C.1.4.5 Interface at 2048 Kbit/s requirements

Table, subclause C.1.4.5

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Interface at 2048 kbit/s	5	N/R	
Electrical characteristics	5.1	I_a and I_b	C.2
Frame structure	5.2	N/R	
Number of bits per timeslot	5.2.1	I_a and I_b	C.2.5.1
Number of time slots per frame	5.2.2	I_a and I_b	C.2.5.2
Assignments of bits in time slot 0	5.2.3	I_a and I_b	C.2.5.3
Timeslot assignment	5.2.4	N/R	
Frame alignment signal	5.2.4.1	I_a and I_b	C.2.5.3.1
D-channel	5.2.4.2	I_a and I_b	C.4.2
B-channel and H-channels	5.2.4.3	I_a and I_b	C.2.6
Bit sequence independence	5.2.4.4	I_a and I_b	C.3.1.1
Timing considerations	5.3	I_a and I_b	C.2.7
Unsynchronized condition		I_a and I_b	C.2.1
Jitter	5.4	N/R	
General considerations	5.4.1	I_a and I_b	C.2.8
Minimum tolerance to jitter and wander at inputs	5.4.2	I_a and I_b	C.2.8.1
TE and NT2 output jitter	5.4.3	N/R	
TE and NT2 with only one user-network interface	5.4.3.1	I_a	C.2.8.2.1
		I_b	C.2.8.2.2
TE with more than one user-network interface to the same network	5.4.3.2	I_a	C.2.8.2.1
		I_b	C.2.8.2.2

continued

Table, subclause C.1.4.5 (continued)

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Tolerable longitudinal voltage	5.5	I_a and I_b	C.2.9
Output signal balance	5.6	N/R	see C.2.10
Impedance towards ground	5.7	I_a and I_b	C.2.11
Interface procedures	5.8	N/R	
Codes for idle channels and idle slots	5.8.1	I_a and I_b	C.4.1
Interframe (layer 2) time fill	5.8.2	I_a and I_b	C.4.2
Frame alignment and CRC-4 procedures	5.8.3	I_a and I_b	C.4.3 C.4.4 C.4.5
Maintenance at the interface	5.9	N/R	
Definitions of maintenance signals	5.9.1	I_a and I_b	C.3.1.2 C.3.1.3 C.3.1.4 C.3.1.5
Use of CRC procedure	5.9.2	N/R	
Introduction	5.9.2.1	I_a and I_b	C.4.4, C.4.5
Localization of the CRC functions in the subscriber access from the user point of view	5.9.2.2	N/R	
No CRC processing in the transmission link	5.9.2.2.1	N/R	
CRC processing in the digital transmission link	5.9.2.2.2	N/R	
Maintenance functions	5.9.3	N/R	
General requirements	5.9.3.1	I_a and I_b	C.3.2

continued

Table, subclause C.1.4.5 (continued)

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Maintenance functions on the user side	5.9.3.2	N/R	
Anomalies and defect detection	5.9.3.2.1	I_a	C.3
Detection of defect indication signals	5.9.3.2.2	I_a	C.3
Consequent actions	5.9.3.2.3	I_a	C.3
Maintenance functions on the network side	5.9.3.3	N/R	
Defect detection	5.9.3.3.1	I_b	C.3
Detection of defect indication signals	5.9.3.3.2	I_b	C.3
TABLE 7/I.431 - Defect conditions and defect indication signals detected by the user side and consequent actions	5.9.3.3.2	I_a	C.3.2.2
Consequent actions	5.9.3.3.3	I_b	C.3
TABLE 8/I.431 - Defect conditions and defect indication signals detected by the network side of interface and consequent actions	5.9.3.3.3	I_b	C.3.2.1

C.1.4.6 Interface connector requirements

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Connector	6	N/R	

C.1.4.7 Interface wiring requirements

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Interface wiring	7	N/R	

C.1.4.8 Power feeding requirements

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Power feeding	8	N/R	
Provision of power	8.1	I_a	C.5.1
Power available at the NT	8.2	I_a I_b	C.5.1 C.5.4
Feeding voltage	8.3	I_a	C.5.1
Safety requirements	8.4	I_a I_b	C.5.2, C.5.3, see ETS 300 046 C.5.4, see ETS 300 046

C.1.4.9 PTNX interconnection requirements

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Application of the ETS for PTNX inter-connections (leased lines)	Annex A A.3.1.1 A.3.2 A.3.3		C.2.1 C.2.7.2 C.2.8.1 C.2.8.2

C.1.4.10 Additional requirements for application at S reference point

Functions	Clause/ subclause	Relevant interface I_a, I_b or I_a and I_b	Test defined in
Application of the ETS to the S reference point	Annex B		
	B.4.1	I_b	C.2.1 C.2.7.2
	B.4.2	I_b	C.2.8.2
	B.4.3	I_a and I_b	C.2.5.3.1, C.3.1.1
	B.5	N/R	
	B.6	I_a	C.3.1.1

C.2 Electrical characteristics tests

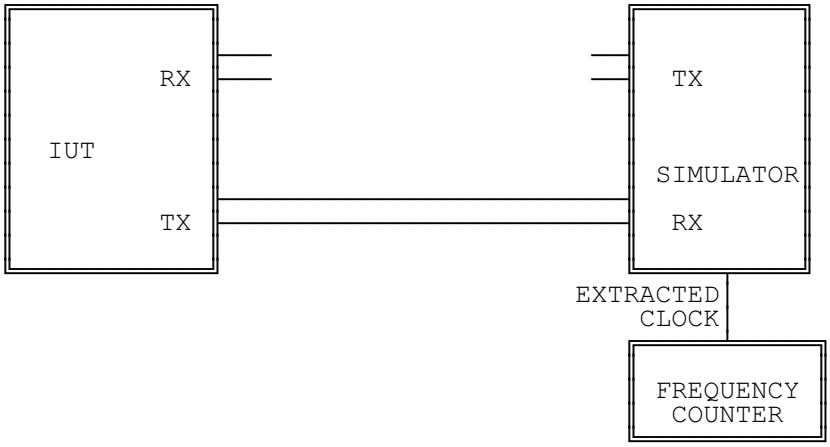
These tests check that the interface conforms to the electrical characteristics specified in table 1, § 5.1.

C.2.1 Bit rate when unsynchronized

Test applicable for I_a and I_b interface.

Purpose: To measure the bit rate when the IUT (Implementation Under Test) is not synchronized.

Test configuration:



System state for I_a: State F3, IUT transmitting RAI.

System state for I_b: State G4, IUT transmitting AIS.

Stimulus: No signal from the simulator to the input supplying timing.

I_a case: interruption of the signal at the T reference point.

I_b case: interruption of the signal at any point between NT1 and ET or at the interface I_a of a PTNX supplying timing.

Monitor: Measure bit rate with frequency counter, as extracted by the timing recovery circuit of the network simulator.

The measurement overall accuracy shall be better than 1% of the bit rate tolerance.

Results: - I_a interface - For IUT as defined in subclause A.3.1.1, foreseen to act as a master, the corresponding bit rate shall be in the range 2048 kbit/s ± 32 ppm, in all other cases the corresponding bit rate shall be in the range 2048 kbit/s ± 50 ppm.

- I_b interface, T reference point - The corresponding bit rate shall be in the range 2048 kbit/s ± 50 ppm.

- I_b interface, S reference point - The corresponding bit rate shall be in the range 2048 kbit/s ± 32 ppm (as defined in subclause B.4.1).

C.2.2 Received and transmitted line code

C.2.2.1 Received line code

Test applicable for I_a and I_b interfaces.

Purpose: To test the line coding of the received frames.

This test is included in test C.4.5 (CRC4 processing).

C.2.2.2 Transmitted line code

Test applicable for I_a and I_b interfaces.

Purpose: To test the line coding of the transmitted frames.

This test is included in test C.3.1.1 (Normal Operational Frame).

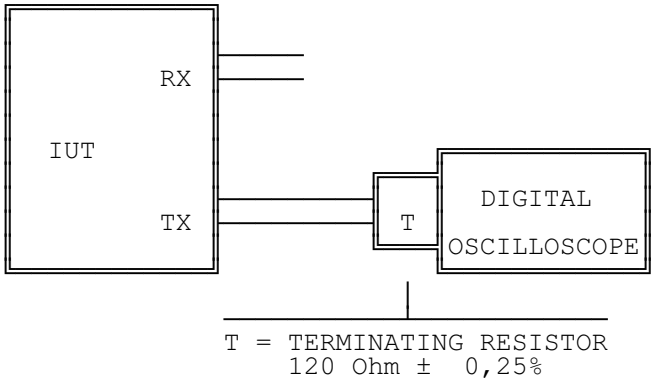
C.2.3 Specifications at the output ports

C.2.3.1 Pulse shape and amplitude of a mark (pulse)

Test applicable for I_a and I_b interfaces.

Purpose: To check the conformance of the shape of all mark pulses, irrespective of the polarity, transmitted by IUT.

Test configuration:



System state for I_a: Any state F1 to F5.

System state for I_b: Any state G1 to G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: The marks transmitted by IUT.

Results: Both positive and negative pulse shall be within the mask of figure 15/CCITT Recommendation G.703 [2], assuming V = 100%, to be 3V.

NOTE 1: The measurement overall accuracy should be better than 1% of the nominal amplitude of a mark (ie. 3V).

NOTE 2: All the measurements should be performed using a digital oscilloscope in DC mode.

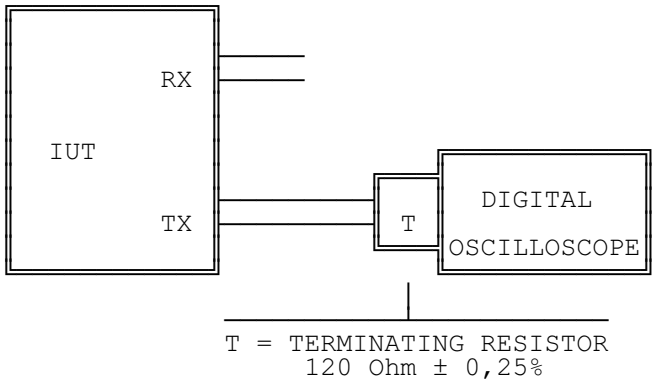
NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependant on the energy of the positive and the negative pulses.

C.2.3.2 Peak voltage of a space (no pulse)

Test applicable for I_a and I_b interfaces.

Purpose: To check the absence of any voltage higher than 10% of the nominal peak value of a pulse during the transmission of a space (no pulse).

Test configuration:



System state for I_a: Any state F1 to F5.

System state for I_b: Any state G1 to G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: The spaces transmitted by IUT.

Results: The bit interval corresponding to a transmission of a space shall not present voltages higher than ± 0,3 V.

NOTE 1: The measurement overall accuracy should be better than 1% of the nominal amplitude of a mark (ie. 3V).

NOTE 2: All the measurements should be performed using a digital oscilloscope in DC mode.

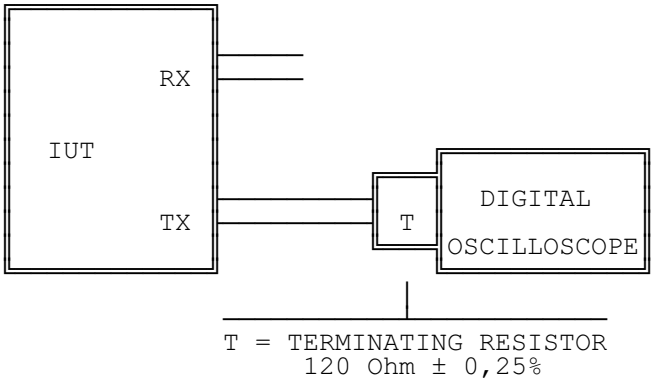
NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

C.2.3.3 Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval

Test applicable for I_a and I_b interfaces.

Purpose: To check the balance between the amplitude of positive and negative pulses (measured at the centre of the pulse interval).

Test configuration:



System state for I_a: Any state F1 to F5.

System state for I_b: Any state G1 to G5.

Stimulus: Relevant signal defined to force IUT to enter the appropriate state.

Monitor: The amplitude of positive and negative pulses (measured at the centre of the pulse interval).

To determine the centre of a pulse:

- Determine the level equal to half the nominal pulse amplitude (i.e. 1,5 V), where the width of the actual pulse shall be measured;
- a point equal to half the value of the measured width of the pulse is the centre of the pulse.

Results: The ratio between the amplitudes shall be within the range from 0,95 to 1,05.

NOTE 1: The measurement overall accuracy should be better than 0,25% of the nominal ratio.

NOTE 2: All the measurements should be performed using a digital oscilloscope in DC mode.

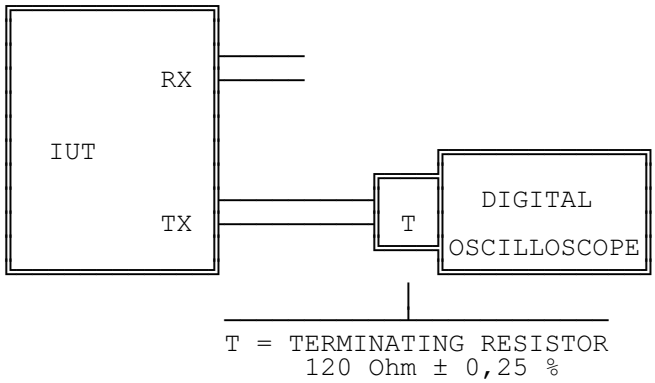
NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

C.2.3.4 Ratio of the widths of positive and negative pulses at the nominal half amplitude

Test applicable for I_a and I_b interfaces.

Purpose: To check the balance between the time duration of pulses of different polarity (measured at the half of the nominal pulse amplitude).

Test configuration:



System state for I_a: Any state F1 to F5.

System state for I_b: Any state G1 to G5.

Stimulus: Relevant signal defined to force IUT to enter the appropriate state.

Monitor: The time duration of positive and negative pulses measured at the nominal half of the pulse amplitude (i.e. 1,5 V).

Results: The ratio between the time durations shall be within the range from 0,95 to 1,05.

NOTE 1: The measurement overall accuracy should be better than 1 % of the nominal ratio.

NOTE 2: All the measurements should be performed using a digital oscilloscope in DC mode.

NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

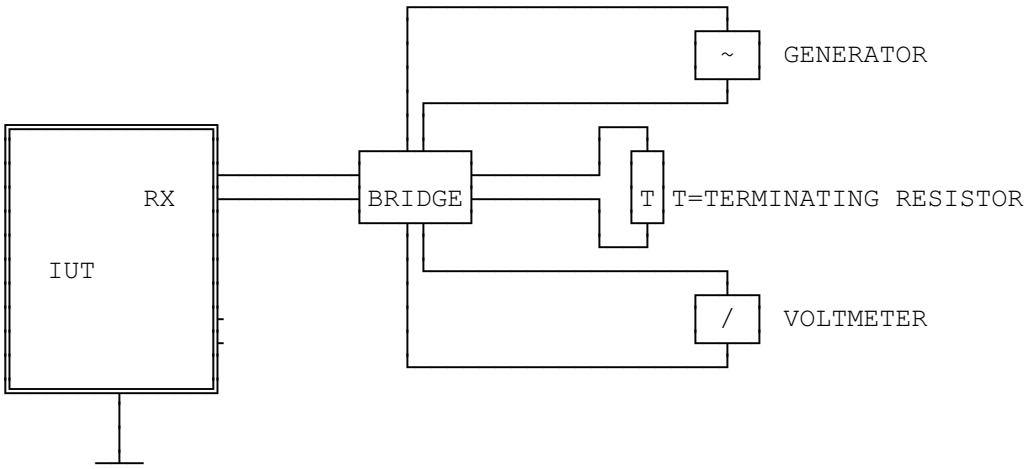
C.2.4 Specifications at the input ports

C.2.4.1 Return loss at the input port

Test applicable for I_a and I_b interfaces.

Purpose: To measure the return loss of the receiving section of IUT.

Test configuration:



System state: Powered.

Stimulus: Sinusoidal signal of 3 V peak at the input port, and frequency variable between 51 kHz and 3072 kHz.

Monitor: Voltage measured across the bridge, representing a terminating resistor of 120 Ohm, using a selective voltmeter with bandwidth less than 1 kHz.

Results: The measured return loss shall comply with the following table:

Frequency range			Return loss
51 kHz	to	102 kHz	12 dB
102 kHz	to	2048 kHz	18 dB
2048 kHz	to	3072 kHz	14 dB

NOTE 1: The characteristics of the generator and of the voltmeter may be different depending on the implementation of the bridge however the total error of the test set-up should be less than 0,5 dB in the range between 10 and 20 db. When connected to a 120 Ohms ± 0,25 % resistor the measured return loss of the bridge should be 20 dB higher than the specified limits for the IUT.

C.2.4.2 Input port immunity against reflections

Test applicable for I_a and I_b interfaces.

Purpose: To check the input port immunity against an interfering signal combined with the input signal with a cable attenuation of maximum 6 dB.

Test configuration:

The output signal of the network simulator shall conform to a pulse shape as defined in figure 15 of CCITT Recommendation G.703 [2] when sending normal operational frames. The binary content of the timeslots 1 to 31 shall comply with the PRBS 2^{15}-1 as defined in CCITT Recommendation O.151 [5].

Due to the lack of definition of the return loss for transmitters in CCITT Recommendation G.703 [2], the simulator output shall provide maximum reflection (i.e. low output impedance to simulate simple transmitter implementations).

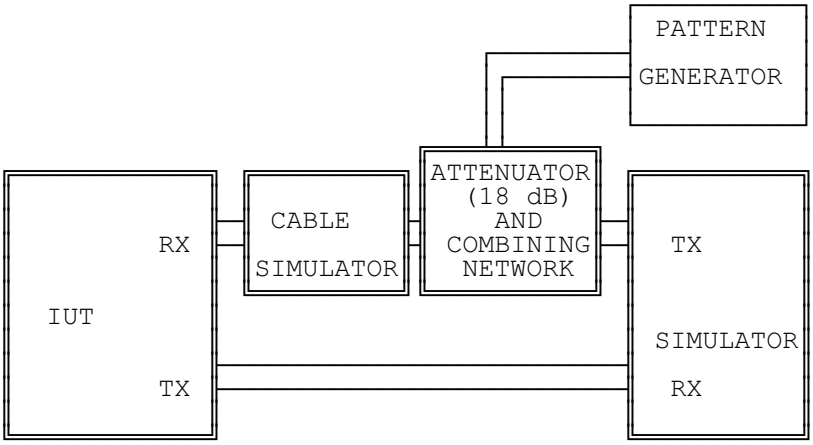
The interfering signal shall conform to a pulse shape as defined in figure 15 of CCITT Recommendation G.703 [2], encoded HDB3. Its binary content shall comply with the PRBS 2^{15}-1 as defined in CCITT Recommendation O.151 [5]. The bit rate shall be within the limits specified in CCITT Recommendation G.703 [2] (± 50ppm) and shall not be synchronised to the output signal of the simulator.

The interfering signal shall be combined with the main signal in a combining network having an impedance of 120 Ohm, with zero loss in the main path and an attenuation of the interference path of 18 dB.

The conformance of IUT must be verified in the following two test conditions:

a) without cable simulator. The amplitude of the signal transmitted by the simulator shall be 3,3 V (nominal amplitude + 10 %);

b) with cable simulator having 6 dB attenuation measured at 1024 kHz and following a ´f law. The amplitude of the signal transmitted by the simulator shall be 2,7 V (nominal amplitude -10 %).



System state for I_a: State F1.

System state for I_b: State G1.

Stimulus: Normal Operational frames with PRBS pattern 2^{15}-1 in timeslots 1 to 31.

PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

The test shall be repeated with the wires at the IUT input reversed.

Monitor: Monitor the CRC error information report transmitted by IUT.

Results: No E bit set to 0 shall be received for a time period of at least one minute.

NOTE 1: The $\sqrt{f}$ law of a cable simulator should apply in a frequency range 100 kHz to 10 MHz.

NOTE 2: This test relies on the correct operation of the CRC error information report by IUT.

C.2.5 Frame structure

These tests check the frame composition.

C.2.5.1 Number of bits per timeslot

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

C.2.5.2 Number of timeslots per frame

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

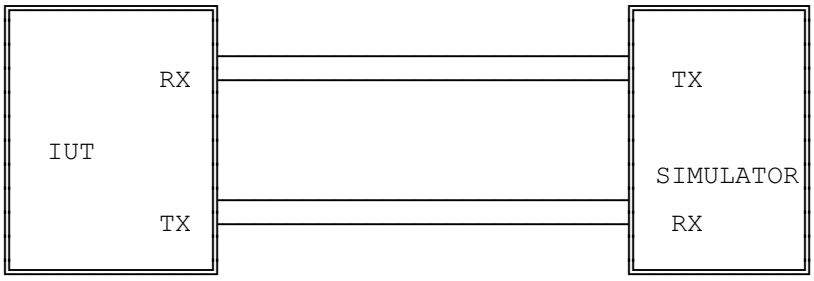
C.2.5.3 Assignment of bits in timeslot 0

C.2.5.3.1 Generation of frame alignment word

Test applicable for I_a and I_b interfaces.

Purpose: To check the correct generation of frame alignment word, multiframe alignment word, CRC bits C1 to C4.

Test configuration:



System state for I_a: Any state F1 to F5.

System state for I_b: State G1, G2, G3, G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: Correct frame alignment word pattern.

Results: No detection of incorrect frame alignment word, multiframe alignment word, and no received submultiframes in error within 1 second measured in any state. For IUT with CRC-DISABLE function activated (as defined in subclause B.4.3) bit 1 of timeslot 0 shall always be ONE.

During this test the E bit is not considered.

C.2.5.3.2 Sa bits

Test applicable for I_a and I_b interfaces.

Purpose: To check the Sa bits contained in timeslot 0 of the frame not containing the frame alignment signal:

- bits 4 and 8 are reserved for international use are not defined;

- bits 5, 6 and 7 are reserved for national use in the access digital section.

Since no specific functions are defined for the Sa bits, no specific test is prescribed for the generation of these Sa bits. The immunity of the receiving side to the Sa bits is implicitly tested with the test described in subclause C.3.2.2.

C.2.6 Timeslot assignment

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

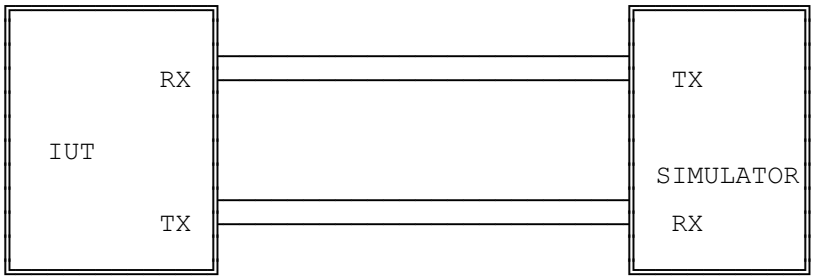
C.2.7 Timing considerations

C.2.7.1 AIS recognition

Test applicable for I_a interface.

Purpose: To check the ability of IUT to recognize AIS.

Test configuration:



System state: State F4.

Stimulus: AIS signal with clock frequency 2048 kbit/s ± 50 ppm.

It is not possible to distinguish between states F3 and F4 using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Monitor: The frames transmitted by IUT.

Results: IUT shall remain in state F4, therefore no change of error indication shall occur.

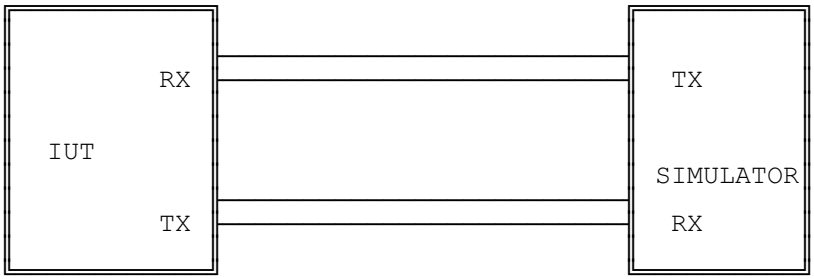
IUT having more than one access shall not synchronize its internal reference clock to the incoming signal frequency.

C.2.7.2 Synchronisation

Test applicable for I_a interface.

Purpose: The ability of IUT to synchronize its timing on the signal received from the network.

Test configuration:



System state: State F1.

Stimulus: Normal operational frames with clock frequency variation from the nominal value:

For IUT to be connected to T reference point the corresponding bit rate shall be in the range 2048 kbit/s ± 5 ppm;

For IUT to be connected to S reference point the corresponding bit rate shall be in the range 2048 kbit/s ± 32 ppm;

For interface at IUT for PTNX interconnection the corresponding bit rate shall be in the range 2048 kbit/s ± 32 ppm.

For implementation with free running clock frequency accuracy better than ± 1 ppm, as declared by the equipment supplier the stimulus shall be in the range ± 1ppm.

In case of Multi Access IUT, this test has to be performed on each access declared to be capable to extract synchronisation from the network, while all other accesses are in state F3 or F4.

The stimulating signal is provided to a timing synchronizing input of IUT. The frequency of the output signal at each access has to follow the input signal frequency.

Monitor: The frames transmitted by IUT.

Results: 1) The IUT shall remain in state F1.

2) The frequency of the outgoing signal at each access has to follow the frequency of the stimulating input signal.

NOTE 1: The speed of the variation of the output frequency depends on the Q factor of the reference clock recovery timing of the IUT.

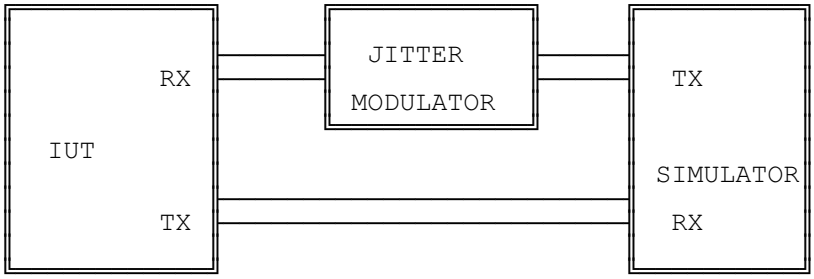
C.2.8 Jitter

C.2.8.1 Minimum tolerance to jitter and wander at inputs

Test applicable for I_a and I_b interfaces

Purpose: To check the ability of IUT to tolerate on the 2048kbit/s incoming signal a sinusoidal jitter/wander in accordance with table 1, subclause 5.4.2.

Test configuration:



System state for I_a: State F1.

System state for I_b: State G1.

Stimulus: Normal Operational frames with jitter/wander according to table 1, subclause 5.4.2. and with a PRBS pattern 2^{15}-1 in timeslots 1 to 31. PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

Other inputs in state F3 (G3 for interface I_b).

This test has to be performed for the following frequencies:

For IUT to be connected to T reference point, simulator providing the nominal frequency plus 5 ppm and minus 5 ppm;

For IUT to be connected to S reference point, simulator providing the nominal frequency plus 32 ppm and minus 32 ppm;

For interface at IUT for PTNX interconnection, simulator providing the nominal frequency plus 32 ppm and minus 32 ppm.

For implementation with free running clock frequency accuracy better than ± 1ppm, as declared by the equipment supplier the stimulus shall be in the range ± 1ppm.

Points A1-f2 and A2-f4 shall be measured. For the range between A0-f0 to A1-f1 the jitter behaviour can be determined from the Q factor.

For I_a interface Multi Access IUT case:

On each access declared to be capable of extracting synchronisation from the network this test shall be performed by imposing a maximum wander of 20,5 UI while all other accesses are in state F3 or F4.

On each pair of accesses declared to be capable of extracting synchronisation from the network, when evaluating the effect of wander, the amount of phase difference (i.e. 20,5 UI) shall be given to each access, but with opposite phase, i.e. the maximum relative phase difference is 41 UI.

An access not declared to be capable of extracting synchronisation from the network the test shall be made in conjunction with an access capable of extracting synchronisation, when evaluating the effect of

wander, the amount of phase difference (i.e. 20,5 UI) shall be given to each access, but with opposite phase, i.e. the maximum relative phase difference is 41 UI.

Monitor: The frames transmitted by IUT.

Results: IUT shall remain in state F1 (G1 for interface I_b), no CRC error information report shall be detected by the simulator.

IUT declared suitable for leased lines applications shall tolerate a jitter A1 of 1,5 UI with corresponding f2 of 2,4 kHz (see subclause A.3.2).

NOTE 1: This test relies on the correct operation of the CRC error information report by IUT.

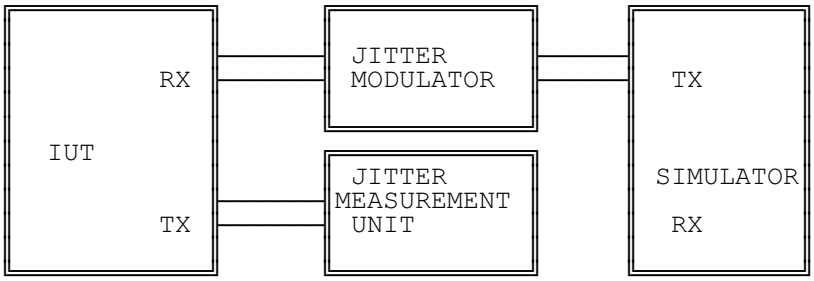
C.2.8.2 Output jitter

C.2.8.2.1 Output jitter with jitter at the input supplying timing

Test applicable for I_a interface.

Purpose: To measure the jitter generated from IUT in the presence of input jitter when IUT is synchronised by the simulator.

Test configuration:



The jitter measurement shall be done using equipment that has an external timing reference to the jitter measurement set which has no phase variation energy in the jitter region under test.

System state: State F1.

Stimulus: Normal operational frames with jitter according to table 1, subclause 5.4.2, provided to the synchronising input and with a PRBS pattern 2^{15}-1 in timeslots 1 to 31. PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

Interface at IUT for PTNX interconnection shall tolerate a jitter A1 of 1,5 UI with corresponding f2 of 2,4 kHz (see subclause A.3.2).

a) For IUT to be connected to T reference point only.

This test shall be performed for three different cases:

1) simulator providing the nominal frequency;

2) simulator providing the nominal frequency plus 5 ppm;

3) simulator providing the nominal frequency minus 5 ppm.

b) For IUT to be connected to S reference point and for IUT used for PTNX interconnections.

This test shall be performed for three different cases:

1) simulator providing the nominal frequency;

2) simulator providing the nominal frequency plus 32 ppm;

3) simulator providing the nominal frequency minus 32 ppm.

For interface at IUT for PTNX interconnection, having implementation with free running clock frequency accuracy better than ± 1ppm, as declared by the equipment supplier, the stimulus shall be in the range ± 1ppm.

Monitor: The jitter extracted from the signal transmitted by the IUT measured at all outputs.

Results: The peak to peak jitter shall comply with the following table:

Measurement filter bandwidth		Output jitter
Lower cutoff (high pass)	Upper cutoff (low pass)	UI peak-to-peak
20 Hz (NOTE1)	100 kHz	1,1 UI (NOTE 3)
400 Hz (NOTE2)	100 kHz	0,11 UI

NOTE 1: In case of Multi Access IUT the lower cutoff frequency shall be 4 Hz.

NOTE 2: In case of Multi Access IUT the lower cutoff frequency shall be 40Hz.

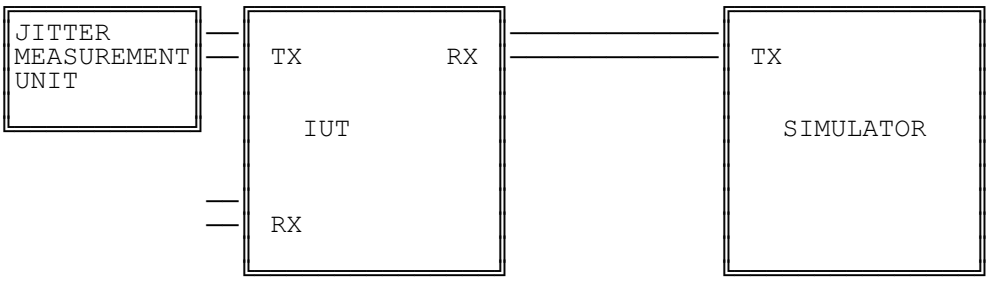
NOTE 3: Interface at IUT for PTNX interconnection shall not exceed 1,6 UI when measured with a lower cut-off (high pass) at 4 Hz high pass (see subclause A.3.3).

C.2.8.2.2 Output jitter at network side

Test applicable for I_b interface.

Purpose: To measure the jitter generated from the IUT.

Test configuration:



The jitter measurement shall be done using equipment that has an external timing reference to the jitter measurement set which has no phase variation energy in the jitter region under test.

System state: State G1.

Stimulus: a) For test at interface at T reference point:

Normal operational frames without jitter provided by the simulator (e.g. connected at V3 reference point to the digital section) and with a PRBS pattern 2^{15}-1 in timeslots 1 to 31. PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

This test shall be performed for three cases:

1) simulator providing the nominal frequency.

2) simulator providing the nominal frequency plus 5 ppm.

3) simulator providing the nominal frequency minus 5 ppm.

b) For test at interface at S reference point:

Normal operational frames with jitter according to table 1, subclause 5.4.2, provided to the synchronizing input of IUT (i.e. I_a interface at T reference point) and with a PRBS pattern 2^{15}-1 in timeslots 1 to 31. PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

This test shall be performed for three cases:

1) simulator providing the nominal frequency.

2) simulator providing the nominal frequency plus 32 ppm.

3) simulator providing the nominal frequency minus 32 ppm.

Monitor: The jitter extracted from the signal transmitted by the IUT.

Results: The peak to peak jitter shall comply with the following table:

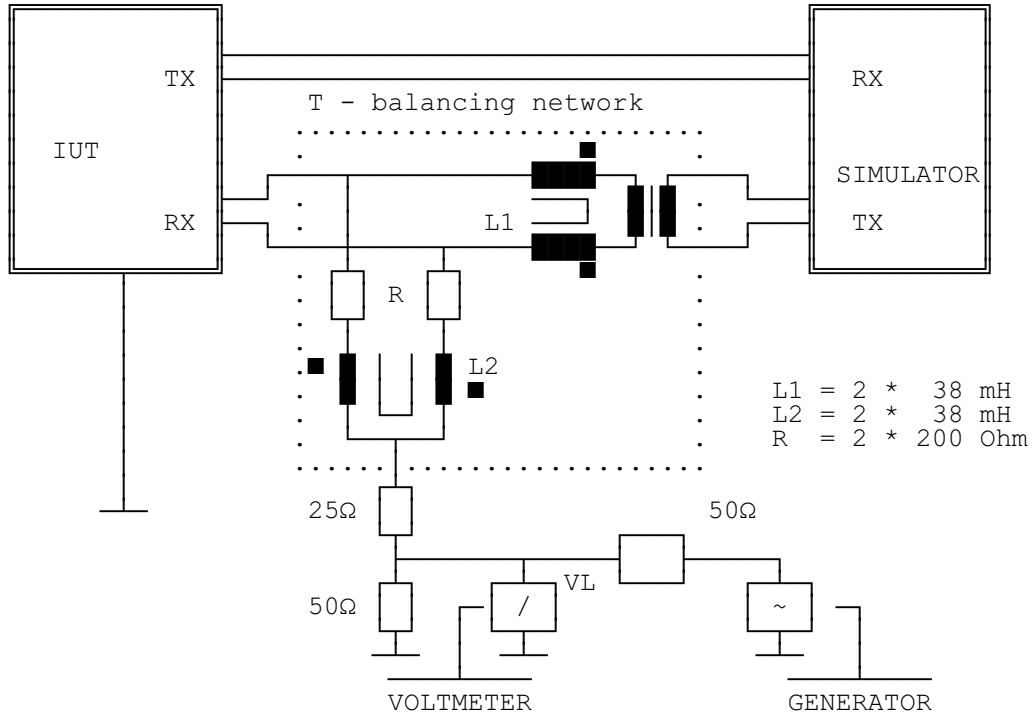
Measurement filter bandwidth		Output jitter
Lower cutoff (high pass)	Upper cutoff (low pass)	UI peak-to-peak
20 Hz	100 kHz	≤ 1 UI
18 kHz	100 kHz	≤ 0,2 UI

C.2.9 Tolerable longitudinal voltage

Test applicable for I_a and I_b interfaces.

Purpose: To check minimum tolerance to longitudinal voltage at input ports.

Test configuration:



NOTE: The transformer has been added to provide earth decoupling between the IUT and the simulator.

System state for I_a: State F1.

System state for I_b: State G1.

Stimulus: Normal operational frames with PRBS pattern 2^{15}-1 in timeslots 1 to 31. PRBS 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

A longitudinal sinusoidal voltage VL of 2Vrms shall be applied for 2 seconds at any frequency chosen in the range 10 Hz - 30 MHz.

Monitor: Frames transmitted by IUT.

Results: IUT shall remain in state F1 (G1 for interface I_b), no CRC error information report shall be detected by the simulator.

C.2.10 Output signal balance

This test is covered by prEN 50096 [7].

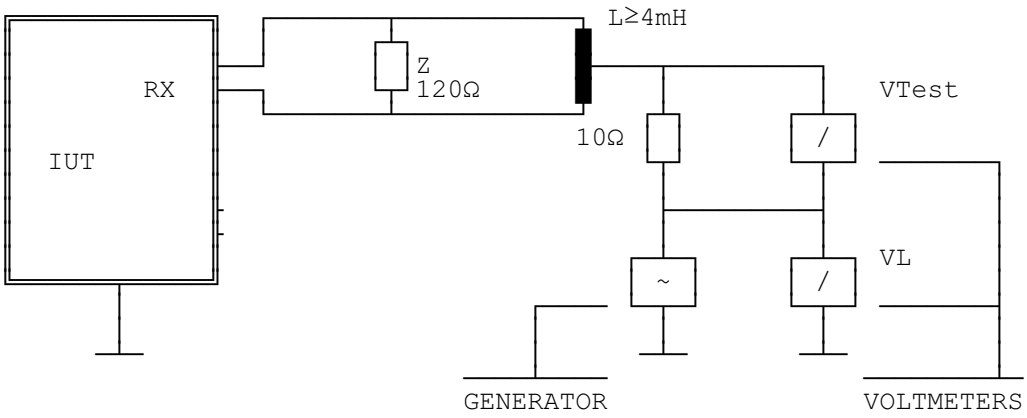
C.2.11 Impedance towards ground

C.2.11.1 Impedance towards ground of the receiver

Test applicable for I_a and I_b interfaces.

Purpose: To check IUT receiver input impedance towards ground.

Test configuration:



System state for I_a: State F3.

System state for I_b: State G5.

Stimulus: Sinusoidal test signal voltage VL shall be 2 Vrms.

The test signal shall be applied at any frequency chosen in the range 10 Hz - 1 MHz.

Monitor: Voltage of VTEST.

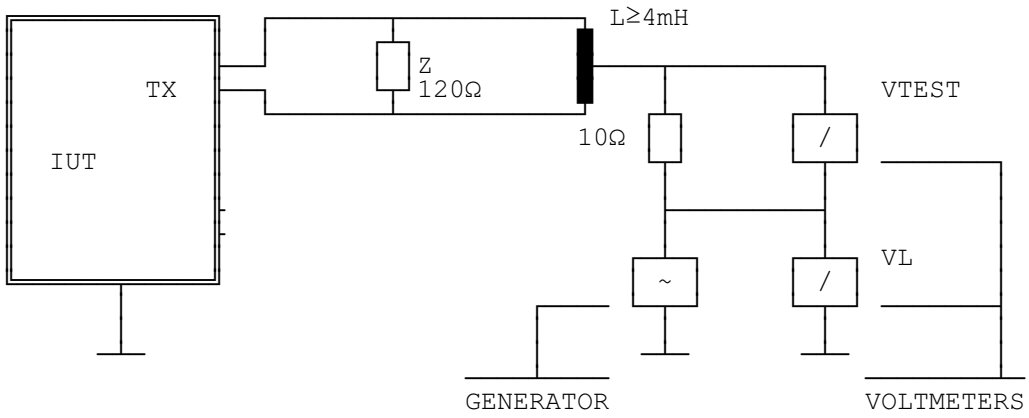
Results: Voltage VTEST ≤ 20 mVrms.

C.2.11.2 Impedance towards ground of the transmitter

Test applicable for I_a and I_b interfaces.

Purpose: To check IUT transmitter output impedance towards ground.

Test configuration:



System state for I_a: State F3.

System state for I_b: State G5.

Stimulus: Sinusoidal test signal voltage VL shall be 2Vrms.

The test signal shall be applied at any frequency chosen in the range 10 Hz - 1 MHz.

Monitor: Voltage of VTEST.

NOTE 1: Frequency selective level measuring equipments should be used. Wideband measuring equipment is not suitable for devices measuring VTEST and VL.

Results: Voltage VTEST ≤ 20 mVrms.

C.3 Functional characteristics tests

These tests are designed to test conformance to the functional characteristics of the layer 1 of primary rate interface.

C.3.1 Test of signals sent by IUT

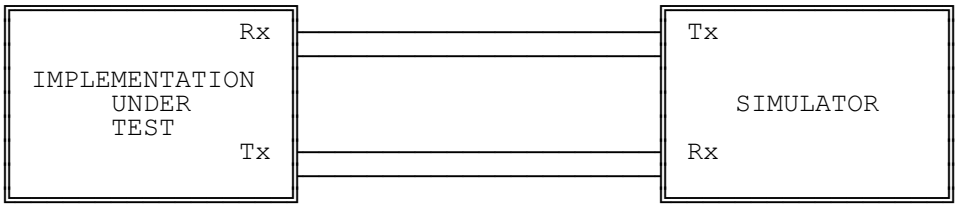
These tests check the different signals sent by the IUT.

C.3.1.1 HDB3 coding and normal operational frame

Test applicable for I_a and I_b interfaces.

Purpose: To check the coding, decoding, and the binary organization of Normal Operational Frame.

Test configuration:



System state for I_a: State F1. Application of one of the facilities defined in subclause C.1.2.1 is required. IUT according to Annex B shall be tested with loopback 4 activated.

System state for I_b: State G1.

Stimulus: Normal Operational Frame sent continuously from the Simulator with valid timeslot 0 including active CRC and without CRC error. Pseudo-random pattern 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1984 kbit/s).

Monitor: The correct coding and the frame structure of the signal sent from the IUT.

Results: The signal received shall be encoded according to the HDB3 coding rule (Annex A of CCITT Recommendation G.703 [2]). The frame shall comprise valid timeslot 0 with A bit set to 0, E bit set to 1 and including correct CRC without CRC blocks in error. For IUT with CRC-DISABLE function activated (as defined in Annex B, subclause B.4.3) bit 1 of timeslot 0 shall always be ONE.

C.3.1.2 Remote alarm indication

Test applicable for I_a and I_b interfaces.

This test is combined with test described in subclause C.3.2

C.3.1.3 Alarm indication signal

Test applicable for I_b interface.

Purpose: To check the correct generation of Alarm Indication Signal (AIS).

This test is combined with test described in subclause C.3.2.

C.3.1.4 CRC error information

Test applicable for I_a and I_b interfaces.

Purpose: To check the detection of CRC blocks in error and the correct report with E bit.

This test is combined with test described in subclause C.4.5.

C.3.1.5 Remote alarm indication and continuous CRC error indication

Test applicable for I_b interface.

Purpose: To check the correct generation of Remote Alarm Indication and Continuous CRC Error Information (RAI and E bit set to ZERO).

This test is combined with test described in subclause C.3.2.

C.3.2 States-matrix at the IUT

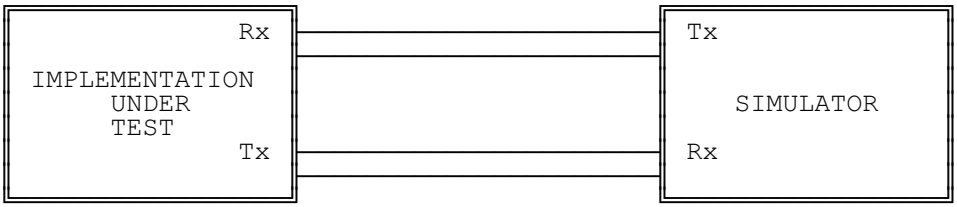
Test applicable for I_b interface.

C.3.2.1 States-matrix at the IUT network side

Test applicable for I_b interface.

Purpose: The tests defined in this subclause intend to check the different stable states at the IUT side and the possible transitions between them. These tests are performed by simulating the opposite side (and simulating internal fault in the IUT for interface I_b), monitoring the IUT at the interface and verifying appropriate state transition.

Test configuration:



System state: Any state G0 to G5.

It is not possible to distinguish between states G1 and G3 using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Stimulus: For each initial state, each possible new event indicated in table 3/I.431 [9] shall be performed, but see also table 1, subclause 3.4.6.

Stimulus shall to be maintained for a time period sufficient to allow the expected state transition.

Sa bits shall be set to binary ONE.

Monitor: The status indication provided by the IUT and the signal transmitted towards the interface.

The final state shall be checked 1 second after the stimulus has been transmitted.

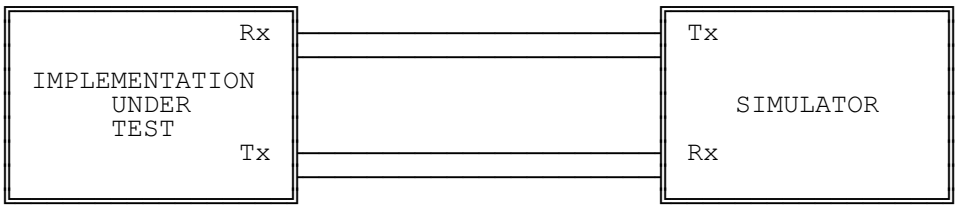
Results: New state, transmitted signal and primitives sent to the higher layers according to table 3/I.431 [9], but see also table 1, subclause 3.4.6.

C.3.2.2 States-matrix at the IUT user side

Test applicable for I_a interface.

Purpose: The tests defined in this subclause intend to check the different stable states at the IUT side and the possible transitions between them. These tests are performed by simulating the opposite side, monitoring the IUT at the interface and verifying appropriate state transition.

Test configuration:



System state: Any state F0 to F5.

It is not possible to distinguish between states F1 , F2 and F5 or between states F3 and F4, using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Stimulus: For each initial state, each possible new event indicated in table 2/I.431 [9] shall be performed, but see also table 1, subclause 3.4.6.

Stimulus shall be maintained for a time period sufficient to allow the expected state transition.

Sa bits in signals having a frame structure shall contain PRBS pattern.

The test shall be made with both signals:

- AIS_2 Sequence of 512 bits composed of 510 ONEs and 2 binary ZEROs. This sequence to check correct AIS recognition according to CCITT Recommendation O.162.

- AIS_3 Sequence of 512 bits composed of 509 ONEs and 3 binary ZEROs. This sequence to check incorrect AIS recognition according to CCITT Recommendation O.162.

Monitor: The status indication provided by the IUT and the signal transmitted towards the interface.

The final state shall be checked 1 second after the stimulus has been transmitted.

Results: IUT shall react on receipt of AIS_3 with state F3.

IUT shall react on receipt of AIS_2 with state F4.

New state, transmitted signal and primitives sent to the higher layers according to table 2/I.431 [9], but see also table 1, subclause 3.4.6.

C.4 Interface procedures tests

Definition of test sequences:

FAS	Frame with correct FAS (Frame Alignment Signal), correct bits C1 to C4 and correct MFAS (CRC Multi Frame Alignment Signal) in timeslot 0.
/FAS	Frame with not correct FAS (Frame Alignment Signal), correct bits C1 to C4 and correct MFAS in timeslot 0.
BIT 2	Bit 2 of timeslot 0 not containing the frame alignment signal.
FRAME A	Two consecutive frames having FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0 and no contiguous group of seven bits which simulates the Frame Alignment Signal in timeslots 1 to 31.
FRAME B	Two consecutive frames having FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0, simulated BIT 2 = 1 in the first timeslot 31 and simulated FAS (no corresponding MFAS) in the second timeslot 31.
FRAME C	Two consecutive frames having /FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0, simulated BIT 2 = 1 in the first timeslot 31 and simulated FAS (no corresponding MFAS) in the second timeslot 31.
SMF A	Sub-multiframe having correct generation of C1 to C4 bits.
SMF B	Sub-multiframe having incorrect generation of C1 to C4 bits.
MF A	Multiframe having correct FAS, BIT 2 = 1, MFAS and correct C1 to C4 bits.
MF B	Multiframe having correct FAS, BIT 2 = 1, but incorrect MFAS and correct C1 to C4 bits.
# n	# indicates that the sequence defined in the previous line may be repeated before entering the next sub-sequence. If the parameter "n" is defined this sequence shall be repeated at least "n" times.

Additional information regarding interface procedure tests for interface I_b.

- When monitoring interface I_b it has to be recognized that a time delay period independent of actual response times of interface receivers/transmitters may be introduced (eg. delays attributable to the implementation of transmission systems between the NT and ET, where a line transmission termination is present or where coding, decoding and processing occurs etc.). Therefore it is to be expected that test state transitions may show a delay when monitored.

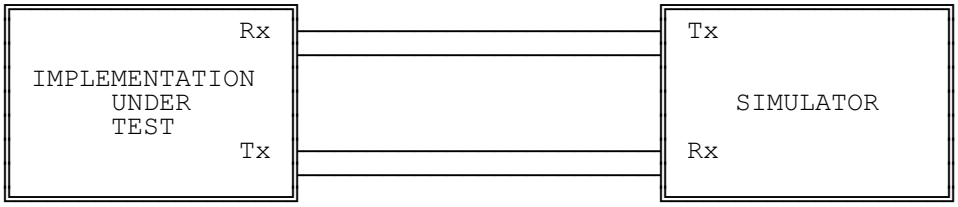
- Separate test response descriptions for interfaces I_a and I_b are provided. Indication of state transition for I_b is given only where stimulus is repeated (indicated by a #). The expected signal response to a repeated stimulus may however still display a time delay.

C.4.1 Codes for idle channels and idle slots

Test applicable for I_a and I_b interfaces.

Purpose: To test the pattern in timeslots which are not assigned to a channel.

Test configuration:



System state for I_a: State F1, no timeslot is assigned to a channel.

System state for I_b: State G1, no timeslot is assigned to a channel.

Stimulus: Normal operational frames from simulator.

Monitor: Pattern in timeslots 1-15 and 17-31 when timeslot 16 is assigned to the D channel.

Pattern in timeslots 1-31 when no D channel is present.

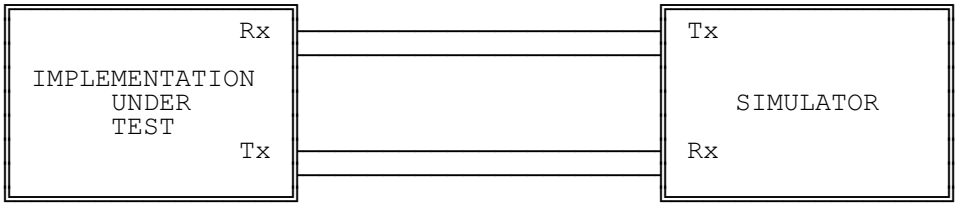
Results: At least three binary ONEs in each timeslot.

C.4.2 Interframe (layer 2) time fill

Test applicable for I_a and I_b interfaces.

Purpose: To test the pattern on the D Channel when the IUT does not send frames.

Test configuration:



System state for I_a: State F1.

System state for I_b: State G1.

Stimulus: Normal operational frames with contiguous HDLC flags in the D-channel from the simulator.

Monitor: Pattern on the D Channel (timeslot 16).

Results: Contiguous HDLC flags.

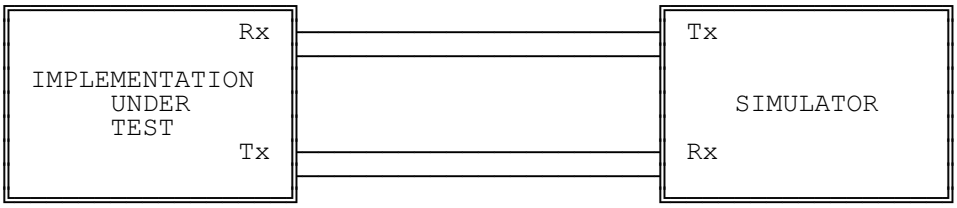
NOTE: An HDLC flag is defined as an octet with a binary pattern 01111110. Therefore contiguous HDLC flags are defined as the consecutive transmission of 8 bit flags. There is no requirement to map the HDLC flag into an octet transmitted in timeslot 16 of one frame.

C.4.3 Frame alignment (without the test of CRC procedure)

Test applicable for I_a and I_b interfaces.

Purpose: To test that IUT correctly executes the frame alignment procedure.

Test configuration:



System state: Various states.

Stimulus: Consecutive correct and bad frame sequences (but including correct multiframe alignment signal and correct bits C1 to C4) from the simulator, i.e. bit 2 to 8 of timeslot 0 containing the frame alignment signal and bit 2 of timeslot 0 not containing the frame alignment signal, as given below.

The test signal shall not contain any other contiguous group of seven bits which simulates the Frame Alignment Signal.

Monitor: Output signal from the IUT.

Results: As listed below.

STIMULUS	MONITOR	COMMENT
BIT 2 = 1, FAS (see *)		
#	NOF	Frame alignment tests
BIT 2 = 1, /FAS	NOF	
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS	NOF	
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1 , /FAS	RAI	
BIT 2 = 1 , FAS, BIT 2 = 1 , FAS	NOF	
#		
BIT 2 = 1 , /FAS, BIT 2 = 1 , /FAS, BIT 2 = 1 , /FAS	RAI	
BIT 2 = 1 , FAS, BIT 2 = 1 , /FAS	RAI	
#		
BIT 2 = 1 , FAS	RAI	
BIT 2 = 0 , FAS	RAI	
#		
BIT 2 = 1 , FAS	NOF	
#		
BIT 2 = 0 , FAS, BIT 2 = 1 , FAS, BIT 2 = 1 , FAS	NOF	
#		
BIT 2 = 0 , FAS, BIT 2 = 0 , FAS, BIT 2 = 1 , FAS	NOF	
#		
BIT 2 = 0 , FAS, BIT 2 = 0 , FAS, BIT 2 = 0 , FAS	RAI or NOF (see **)	
#		
BIT 2 = 1 , FAS	NOF	
#		
BIT 2 = 1 FRAME B	NOF	correct frame alignment
#		
6 X FRAME C	RAI -> NOF	Loss of frame alignment and frame alignment with simulated frame alignment word.
FRAME B	NOF	
#		
4 to 8 mS ——> ▌ RAI and back to NOF will occur (if Multi-Frame Alignment is operating properly), (see ***).		No multiframe alignment on the simulated frame alignment word
No further RAI shall occur within a time period of 20 ms		

* This stimulus shall be repeated in order to allow clock synchronisation of the IUT, the time taken to synchronise may be dependant on the implementation.

** RAI or NOF depending on the implementation options described in CCITT Recommendation G.706 [4].

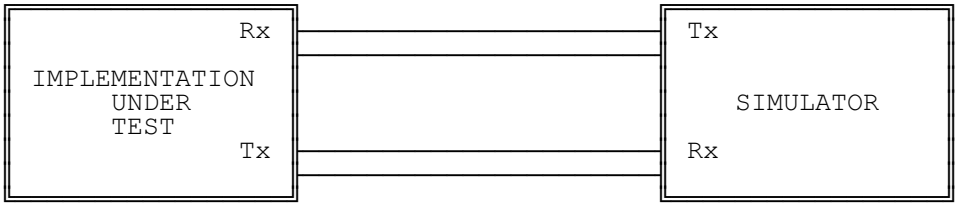
*** The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

C.4.4 CRC multiframe alignment

Test applicable for I_a and I_b interfaces.

Purpose: To test the IUT correctly executes the CRC multiframe alignment.

Test configuration:



System state: Various states.

Stimulus: Consecutive correct and bad CRC multiframe alignment signals from the simulator, i.e. bit 1 in frames not containing the frame alignment signal as given below.

Monitor: Output signal from the IUT as given below.

Results: As listed below.

STIMULUS	MONITOR	COMMENT
FRAME B	(see *)	
#	NOF	
/FAS,BIT 2 = 1,/FAS,BIT 2 = 1		
/Fas,BIT 2 = 1	RAI	Initial condition
MF A	NOF	
4 X MF B	RAI	No multiframe alignment
MF A	NOF	
40 X MF B	NOF, transition to RAI and back to NOF (see **)	2 MFAS within 8ms in the limit of 100ms
MF A, MF B, MF A	NOF	
MF B	NOF	
# 251	Stable NOF	No RAI 500ms after a loss of multiframe alignment
/FAS,BIT 2 = 1,/FAS,BIT 2 = 1		
/FAS,BIT 2 = 1	RAI	Initial condition
MF B	NOF	Correct frame alignment but not multiframe alignment
# 250		No multiframe alignment
MF B	RAI	within 500ms
MF A, 4 X MF B	RAI	
MF A, 2 X MF B, MF A		Undefined condition
MF A, 2 X MF B, 2 X MF A	NOF	Multiframe alignment reached
MF B, MF A	NOF	
#		

* This stimulus shall be repeated in order to allow clock synchronisation of the IUT, the time taken to synchronise may be dependant on the implementation.

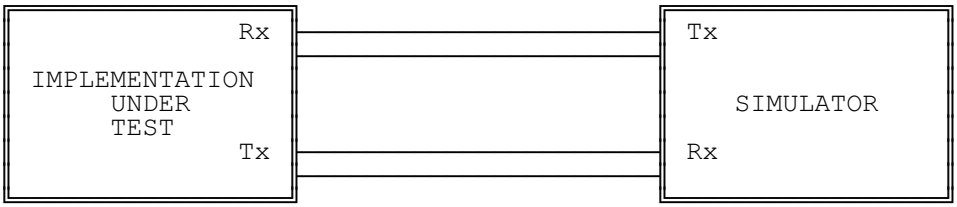
** RAI or NOF depending on the implementation options described in CCITT Recommendation G.706 [4].

C.4.5 CRC processing

Test applicable for I_a and I_b interfaces.

Purpose: To test the correct execution of CRC calculation, comparison with the received bits C1 to C4 and generation of the CRC error report with bit E.

Test configuration:



System state for I_a: State F1.

System state for I_b: State G1.

Stimulus: SMF A and SMF B as given below.

Monitor: Output signal, i.e. E bits as given below.

Results: As listed below.

A CRC error report, indicated by an E bit set to ZERO, shall be received within one second after the generation of a SMF in error. Definition of a SMF in error is given in CCITT Recommendation G.704 [3], subclause 2.3.3.5.3.

STIMULUS	MONITOR			
	I_a	I_b option 1 (NOTE 2)	I_b option 2 (NOTE 2)
SMF A # Repeat more than 1 second	No E bit set to zero	=	=
SMF B	One E bit set to zero	=	=
SMF A #	No E bit set to zero	=	=
SMF B, SMF B	Two contiguous E bits set to zero	=	=
SMF A # Repeat more than 1 second	No E bit set to zero	=	=
914 X SMF B 86 X SMF A	914 contiguous E bits set to zero	=	=
914 X SMF B	914 contiguous E bits set to zero	=	=
SMF A # Repeat more than 1 second	No E bit set to zero	=	=
915 X SMF B 85 X SMF A	| Temporarily RAI (NOTE 3)	=	=
915 X SMF B	|	(NOTE 1)	(NOTE 1)
SMF A #	NOF, no E bit set to zero	=	=
/FAS,BIT 2 = 1,/FAS,BIT 2 = 1, /FAS,BIT 2 = 1	RAI, no E bit set to zero	=	E bit set to 0 plus RAI
#	RAI, no E bit set to zero	=	E bit set to 0 plus RAI

NOTE 1: Due to possible delay temporary RAI may not be detected at I_b.

NOTE 2: Monitor for I_b option 1 and option 2 is considered to be the same as for I_a case (=) unless otherwise stated.

NOTE 3: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

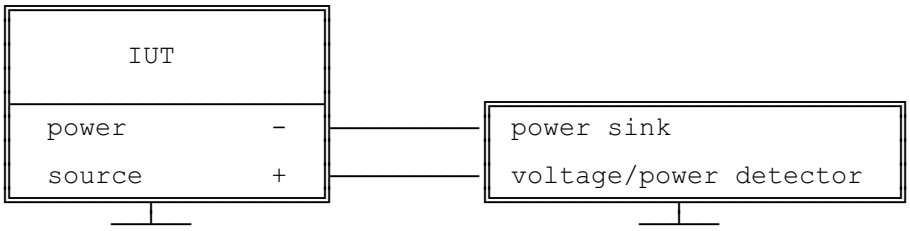
C.5 Power feeding

C.5.1 Provision of power and feeding voltage

Test applicable for I_a interface.

Purpose: To test the provision of power by the IUT.

Test configuration:



System state: Any state F1 to F6.

Stimulus: Power on at IUT; test power sink connected to power interface.

Result: Open circuit voltage: Within the range of - 20 volts to - 57 volts. The voltage, when power up to 7 watts is drawn by the power sink shall be in the range of - 20 volts to - 57 volts.

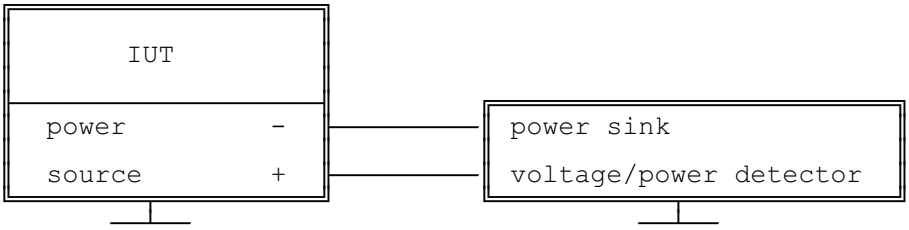
If one of the wires is connected to ground then the polarity of the other wire relative to ground shall be negative.

C.5.2 Protection against short circuit

Test applicable for I_a interface.

Purpose: To verify the ability of the power source to withstand a short circuit condition.

Test configuration:



System state: Any state F1 to F5.

Stimulus: 1) Load equal to 7 watts.

2) Short circuit (5 minutes).

3) Load equal to 7 watts.

4) Wait one minute.

Result: Output voltage after step 4) shall be in the range -20 volts to -57 volts.

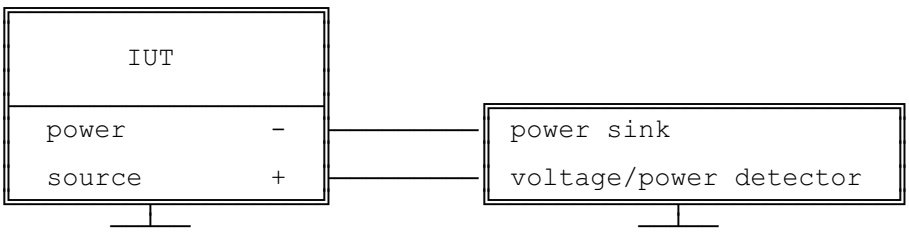
NOTE: The replacement of a broken fuse is permissible.

C.5.3 Protection against overload

Test applicable for I_a interface.

Purpose: To verify the ability of the power source to withstand an overload condition.

Test configuration:



System state: Any state F1 to F5.

Stimulus: 1) Load equal to 7 watts, measure the voltage.

2) Increase the load for 5 minutes to 10,5 watts calculated with the voltage measured in step 1.

3) Load as in step 1 for 1 minute.

4) Load equal to 7 watts.

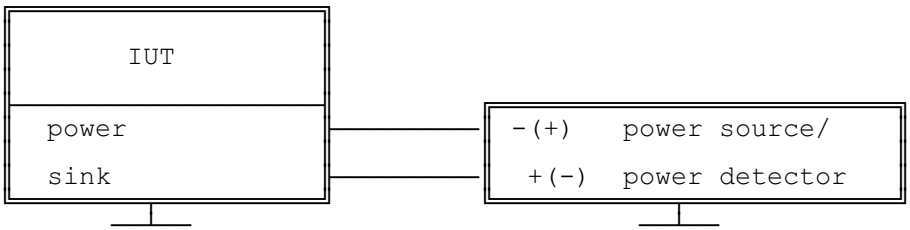
Result: Output voltage after step 4) shall be in the range -20 to -57 volts.

C.5.4 Power consumption and interchange of wires

Test applicable for I_b interface.

Purpose: To verify that the power consumption is within the specified limits and that no damage shall occur in case of interchange of the power feeding wires.

Test configuration:



System state: Any state G1 to G5.

Stimulus: 1) Feeding voltage - 20 volts to - 57 volts (1 minute).

2) Feeding voltage + 20 volts to + 57 volts (5 minutes).

3) Feeding voltage - 20 volts to - 57 volts.

Result: The power drawn by IUT shall not exceed 7 watts. IUT shall be able to operate correctly when fed in step 1 and 3.

Annex D (informative): Characteristics of loopbacks

D.1 Introduction

ETR 001 [14] defines loopbacks used in the maintenance of the customer installation and subscriber access, respectively. This information is repeated here to aid in understanding the layer 1 maintenance capabilities that may affect the user-network interface.

D.2 Characteristics of loopback at the network side

Table D.1: Characteristics of the loopback 2 for primary rate customer access

Loop-back	Location	Channel (s) looped back	Loop back type	Control point	Control mechanism	Application	Implementation
2	in NT1 as near as possible to T towards ET(NOTE2)	Complete loopback	Complete transparent (NOTE 3)	FFS	Layer 1 signals (NOTE 1) (NOTE 2)	Failure localisation + verification	Optional

NOTE 1: These layer 1 signals may not be in the frame signals. They may be line signals.

NOTE 2: In the case of using existing digital transmission systems, a manual loopback may be put in place of the loopback 2, this manual loopback may be implemented between NT 2 and NT 1 and controlled by the user on demand of the network staff.

NOTE 3: The network shall indicate the loss of layer 1 capability of the access during peration of the loopback by transmission of RAI towards the TE. In case of option 2 applied in the NT1 CRC error information towards the TE shall be suppressed (set E-bits towards TE to 1).

D.3 Characteristics of loopbacks for primary rate customer installations

Table D.2: Characteristics of loopbacks for primary rate customer installations

Loop-back	Locations	Channel (s) looped	Loopback type	Control point	Control mechanism	Implementation
B2	Inside the NT2 at the network side	These loopbacks are optional in the TE. When used (e.g. as part of an internal test), the TE should not transmit signal which interferes with the network (i.e. it shall not send operational frames).				
A	Inside the TE					
3	In NT2 as near as poss. to ref. point S towards the T-ref point	30 B&D or 31B channels	complete transparent or non transparent (see note to ETR 001)	NT2	Local maint.	(NOTE 2) optional
				NT2	Layer 3 messages in D-channel or inband signal in B-channel (NOTE 1)	
4	inside the TE	B1 .. B30 (NOTE 3)	partial, transparent or non-transparent	(NOTE 4)	Layer 3	(NOTE 5) optional

NOTE 1: Activation/deactivation of loopback 3 may be requested from a maintenance service provider. The test, however, is performed by the NT2.

NOTE 2: From a technical viewpoint, it is desirable that loopback 3 always be implemented (though it is not mandatory) and so the design of protocols for loopback control should include the operation of loopback 3.

NOTE 3: B-channel loopbacks are controlled by separate control signals. However more than one loopback may be applied at the same time.

NOTE 4: Control by NT2, local exchange, remote maintenance server or remote user.

NOTE 5: The implementation status refers to the equipment for connection to the interface at the T reference point. For equipment for connection to the interface at the S reference point the implementation shall be mandatory according to Annex B (B.6) of this ETS.

Annex E (informative): Bibliography

ECMA 104: "Physical Layer at the Primary Rate Access Interface between Data Processing Equipment and Private Switching Networks".

CCITT Recommendation O.9 (1988): "Measuring arrangements to assess the degree of unbalance about earth".

CCITT Recommendation G.811 (1988): "Timing requirements at the outputs of reference clocks and network nodes suitable for plesichronous operation of international digital links".

CCITT Recommendation G. 823 (1988): "The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy".

CCITT Recommendation O.171 (1988): "Timing jitter measuring equipment for digital systems".

CCITT Recommendation O.162 (1988): "Equipment to perform in-service monitoring on 2048 kbit/s signal".

CCITT Recommendation I.451: "ISDN, user-network interface layer 3 specification for basic call control".

ETS 300 102, part 1: "Integrated Services Digital Network (ISDN); User-Network interface layer 3; Specifications for basic call control.

CCITT Recommendation X.200 (1988): "Reference model of open systems interconnection for CCITT applications.

History

Document history	
April 1992	First Edition
December 1995	Converted into Adobe Acrobat Portable Document Format (PDF)