EUROPEAN TELECOMMUNICATION STANDARD

ETS 300 012

April 1992

Source: ETSI TC-TM

Reference: DE/TM-3009

ICS: 33.040, 33.040.50, 33.080

Key words: ISDN, user network interface, testing

Integrated Services Digital Network (ISDN); Basic user-network interface Layer 1 specification and test principles

ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE
Office address: 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
X.400: c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

Contents

Foreword

This European Telecommunication Standard (ETS) was produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS aims to meet urgent requirements of network operators and equipment manufacturers who are designing equipment to operate with an Integrated Services Digital Network (ISDN) basic rate access user-network interface. This ETS shall replace CEPT Recommendation T/L 03-07 (November 1987).

This ETS takes into account the special requirements from ECMA Standard 103: "Physical layer at the basic access interface between data processing equipment and private switching networks" (1987, 2nd Edition) in Annex B.

Blank page

1 Scope

This European Telecommunication Standard (ETS) specifies requirements and test principles for the ISDN basic rate user-network interface including the physical, electrical and functional characteristics and the information exchange with higher layers. This ensures that interface implementations in an ISDN equipment for use with ISDN basic access is portable within Europe with regard to layer 1 interface aspects and that interworking with higher layer protocols for ISDN is supported.

This ETS is applicable to equipment having interface I_a or I_b for the connection to the ISDN basic access intended to be installed on customers premises. According to CCITT Recommendation I.411 [1], this ETS is to be applied to interfaces at reference points S, T and S/T (coincident S and T) of the ISDN reference configuration.

For the case where this ETS is applied to the T and the S/T reference point, the main body of this text and Annexes A, D and E are normative.

For the case where this ETS is applied to the S reference point, the main body of this text and Annexes A, B, D and E are normative.

This ETS is based on CCITT Recommendation I.430 [2] and gives further requirements or modifications to this base document. Furthermore, this ETS identifies for each aspect defined in CCITT Recommendation I.430 [2] whether it is regarded as normative or informative in the sense of this ETS.

Annexes D and E to this ETS specify the relevant test principles to verify the requirements and for testing conformance to this ETS. It is outside the scope of this ETS to define the static conformance requirements an equipment has to meet for approval attachment to a public network.

This ETS does not specify:

- safety requirements;
- interface or equipment overvoltage protection requirements;
- immunity requirements against electromagnetic interferences;
- emission limitation requirements.

2 Normative references

This European Telecommunication Standard incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to, or revisions of, any of these publications apply to this European Telecommunication Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation I.411, (1988): "ISDN user-network interfaces - reference configurations".

[2] CCITT Recommendation I.430, (1988): "Basic user-network interface - layer 1 specification".

[3] ETS 300 125 (1991): "Integrated Services Digital Network (ISDN); User-network interface data link layer specification, Application of CCITT Recommendations Q.920/I.440 and Q.921/I.441".

[4] prEN 28 877: "Interface connector and contact assignments for ISDN basic access interface located at reference points S and T".

[5] ENV 41 001: "ISDN connector up to 8 pins and up to 2,048 Mbit/s".

[6] prEN 50096: "Integrated Services Digital Network (ISDN); Equipment with ISDN user-network interface at basic and primary rate - EMC requirements".

[7] Final draft prETS 300 047: "Integrated Services Digital Network (ISDN); Basic Access - safety and protection".

[8] CEN/CENELEC ENV 41 004: "Reference Configuration for Calls, based on ISDN Connection Types, as provided by Private Telecommunication Network Exchange".

[9] CCITT Recommendation X.200 (1988): "Reference model of open systems interconnection for CCITT applications".

[10] CCITT Recommendation I.431 (1988): "Primary rate user-network interface - Layer 1 specification".

[11] CCITT Recommendation G.960 (1988): "Digital section for ISDN basic rate access".

[12] CCITT Recommendation G.961 (1988): "Digital transmission system on metallic local lines for ISDN basic rate access".

[13] ETS 300 102-1 (1990): "Integrated Services Digital Network (ISDN); User-network interface layer 3; Specifications for basic call control".

[14] CCITT Recommendation O.171 (1988): "Timing jitter measuring equipment for digital systems".

[15] CCITT Recommendation Q.512 (1988): "Exchange interfaces for subscriber access".

[16] CCITT Recommendation G.812 (1989): "Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links".

3 Definitions

For the purposes of this ETS the following definitions, together with those given in Annex E of CCITT Recommendation I.430 [2] and in CCITT Recommendation I.411 [1] apply.

Terminal equipment (TE): an equipment with interface I_a and consisting of one or more functional blocks.

NOTE: This term is used in this ETS to indicate terminal-terminating aspects of TE1, TA and NT2 functional groups, where these have an I_a interface.

Terminal equipment type 1 (TE1): this functional group includes functions belonging to the functional group TE, and with an interface that complies with the ISDN user-network interface recommendation.

Network termination (NT): an equipment providing interface I_b.

NOTE: This term is used in this ETS to indicate network-terminating aspects of NT1, NT2 and PS1 functional groups where these have an I_b interface.

Network termination type 1 (NT1): this functional group includes functions broadly equivalent to layer 1 (physical) of the OSI reference model. These functions are associated with the proper physical and electromagnetic termination of the network. NT1 functions are:

- line transmission termination;
- layer 1 maintenance functions and performance monitoring;
- timing;
- power transfer;
- layer 1 multiplexing;
- interface termination, including multidrop termination;
- employing layer 1 contention resolution.

Network termination type 2 (NT2): this functional group includes functions broadly equivalent to layer 1 and higher layers of the CCITT Recommendation X.200 [9] reference model. PABXs, local area networks, and terminal controllers are examples of equipment or combinations of equipment that provide NT2 functions. NT2 functions include:

- layer 2 and 3 protocol handling;
- layer 2 and 3 multiplexing;
- switching;
- concentration;
- maintenance functions;
- interface termination and other layer 1 functions.

Terminal adapter (TA): an equipment with interface I_a and one or more auxiliary interfaces that allow non-ISDN terminals to be served by an ISDN user-network interface (see also CCITT Recommendation I.411 [1]).

Power source 1 (PS1): power source for the provision of remote power feeding of TE from NT via a phantom circuit of the interface wires.

Interface I_a: user side of the ISDN user-network interface for the basic access.

Interface I_b: network side of the ISDN user-network interface for the basic access.

4 Abbreviations and symbols

For the purpose of this ETS the following abbreviations apply.

APS:	Auxiliary Power Source
C:	Capacitance
CCITT:	International Telegraph and Telephone Consultative Committee
DC:	Direct Current
ECMA:	European Computer Manufacturers' Association
EMC:	ElectroMagnetic Compatibility
ETS:	European Telecommunication Standard
ETSI:	European Telecommunications Standards Institute
I:	current
I_a:	Interface point a
I_b:	Interface point b
ISDN:	Integrated Services Digital Network
L:	inductance
NT:	Network Termination
PABX:	Private Automatic Branch Exchange
PS:	Power Source / power Sink
R:	Resistor
TA:	Terminal Adaptor
TE:	TErminal
TM:	ETSI Transmission and Multiplexing Technical Committee
V:	Voltage.

5 Conformance

Conformance to this ETS implies that the requirements in normative Clauses/subclauses of this ETS are met when tested according to the test principles given in Annexes D and E, with the exception that the items given in table 1 are optional.

Table 1: Implementation options

Clause/ subclause	Option
7.1.4.2	Power source characteristic a) or b)
7.1.4.4.2	Maximum number of terminals to be fed from power source 1
7.3.1	Maximum number of terminals to be fed from APS, loading factor of APS
7.4	NT1 designed to be compatible with an APS: yes, no
7.4.1	NT1 normal mode voltage detector: yes, no
A.4.4	Connection of NT to user premises wiring
A.4.5	-Connection of the connecting cord to equipment -Location of the terminating resistor at the NT side -Connecting cord is part of TE, or TE is designed for use with "standard ISDN basic access TE cord"
A.5.3.2	-Connected/disconnected indication: a) or b)
A.6.1.4	Priority class: fixed or under control of layer 2
A.6.2.2	TE not able to initiate activation: yes, no
A.6.2.3.2	Activation/deactivation procedure according to table 5, table C-1 or table C-2/I.430 [2]: -TE powered from power source 1 or 2, -TE locally powered and unable to detect PS 1 or 2, -TE locally powered and able to detect PS 1 or 2
A.6.2.4.1 (Table 6)	Timer T2 in NT = 25 ms to 100 ms or T2 = 0
A.6.3.3	TE supporting multiframing: yes, no. NT2 providing multiframing: yes, no.
A.8.6.2	NT designed for configurations according 8.6.2.2, 8.6.2.3, 8.6.2.4 or 8.6.2.5
A.8.6.3	NT designed for round trip delay according 8.6.3.1, 8.6.3.2, 8.6.3.3 or 8.6.3.4
A.8.9	Standard cord length: a) < 7 m or b) 7 m to 10 m
A.9.1.2	-Provision of power source 1 (normal): integral part of NT or physically separated (APS) -Provision of power source 2: yes, no -Provision of power sink 1: yes, no -Provision of power sink 2: yes, no
A.9.2.1	Power available from power source 1
A.9.5.2.1	TE designed for restricted power operation: yes, no
Annex C	TE designed to minimise power disturbance: yes, no

6 Requirements

The requirements in this ETS are given in CCITT Recommendation I.430 [2] together with the statements, modifications and additional requirements as defined in Annex A.

References in CCITT Recommendation I.430 [2] to CCITT Recommendations I.440 or I.441 Annex F candidates shall be read as to ETS 300 125 [3].

7 Additional requirements

The following requirements for dynamic power feeding characteristics are additional to those given in CCITT Recommendation I.430 [2]. They are currently under consideration in CCITT for inclusion into Recommendation I.430 [2].

7.1 Limitations on power source and sink during transient conditions

7.1.1 Current/time limitations for TEs

To limit the current that each terminal can sink from the phantom circuit when connected to PS1 in the normal condition, or when PS1 changes from restricted to normal condition, the terminal shall conform to the mask given in figure 2, with the values given in the table 2, when tested in accordance with figure 1 (for TEs designed to minimise power disturbance see also Annex C).

Table 2: Parameters for the normal condition

A	5 µs	Y	55 mA
C	100 ms	X	current equivalent to 1 Watt never exceeding 55 mA independent of the input voltage

To limit the current that a designated terminal can sink from the phantom when connected to PS1 in the restricted condition, a designated terminal shall conform to the mask given in figure 2, with the values given in table 3, when tested in accordance with figure 1.

Table 3: Parameters for the restricted condition

A	5 µs	Y	55 mA
C	100 ms	X	current equivalent to 380 mW never exceeding 55 mA independent of the input voltage

To limit the current that a non-designated terminal can sink from the phantom when connected to PS1 in the restricted condition a non-designated terminal shall conform to the values given below, when tested in accordance with figure 1.

The power consumption for TEs with connection detector when measured 100 µs after closing the switch shall be ≤ 3 mW.

These TEs shall not assume disconnection (transition from any of the states F2 to F8 to state F1) until the voltage of the interface has remained below 24 V for at least 500 ms.

The current consumption for TEs without connection detector when measured 100 µs after closing the switch shall be ≤ 10 µA.

NOTE: The total effective capacitance at the PS1 input to the TE is expected to be less than 100 µF under all conditions of normal operation, startup and switch-over between normal and restricted mode, or vice versa.

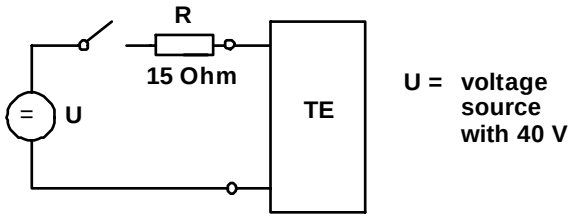


Figure 1: Test circuit to figure 2

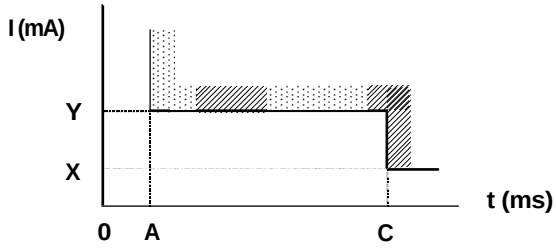


Figure 2: Current/time limitation for TEs

7.1.2 Power source switch-over

7.1.2.1 Power source switch-over time

When changing from normal to restricted mode, or from restricted to normal mode, the transition of the voltage between + 34 V and - 34 V (or vice versa) shall be less than 5 ms. This time is measured with fixed resistive loads, for both normal and restricted power condition, connected to the source, with diodes where necessary. The values of the resistors shall be chosen so that the load draws 420 mW in restricted and n x 1 Watt in normal condition when the source voltage is at its nominal operating value.

7.1.2.2 Restricted mode power source requirements under overload conditions

After the switch-over from normal mode to the restricted mode the power source shall provide a minimum current of 9 mA when the voltage is forced to a level below 1 V (overload condition).

After the switch-over from normal mode to the restricted mode the power source shall be able to provide a minimum current of 11 mA when the source voltage is forced to 34 V.

For conformance test purposes the current shall be measured with a load resistor applied for at least 1 second.

7.1.3 Other TE requirements

7.1.3.1 Minimum TE start up current

A TE designed to operate in restricted power mode shall be able to reach operational condition. In order to check the operational condition INFO 2 is fed permanently at the input of the TE. Operational condition is considered to be reached when the TE starts to send INFO 3. This shall occur when connected to the test circuit given in figure 3, using the parameters given in table 4.

Table 4: Parameters for restricted mode

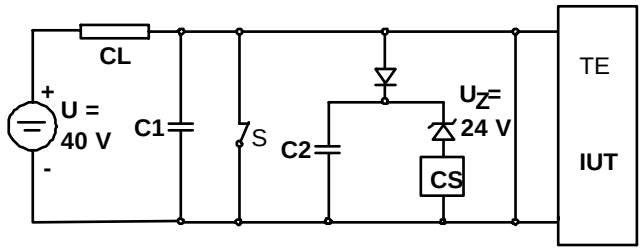
Test a	CL= 9 mA	C1= 0 µF	C2=0 µF	CS=0 mA
Test b	CL=11 mA	C1=300 µF	C2=0 µF	CS=0 mA

CL: current limitation
CS: current sink

A TE designed to operate in normal power mode shall be able to reach operational condition. In order to check the operational condition INFO 2 is fed permanently at the input of the TE. Operational condition is considered to be reached when the TE starts to send INFO 3. This shall occur when connected to the test circuit given in figure 3, using the parameters given in table 5.

Table 5: Parameters for normal mode

Test a	CL = 72 mA	CS = 45 mA
	C1 = 0 µF	C2 = 300 µF
Test b	CL = 72 mA	CS = 45 mA
	C1 = 300 µF	C2 = 300 µF



UZ: zener voltage

Figure 3: Power start up test for TE

7.1.3.2 Protection against short term interruptions

A TE shall not lose an on-going communication when the provision of power in normal or restricted power mode is interrupted for less than, or equal to, 5 ms.

7.1.3.3 Behaviour at the switch-over

A designated TE being in normal mode may change to the restricted mode condition including power consumption limitation immediately after detection of an interruption of power (in order to protect an on-going communication by reducing its power consumption).

When the change from normal mode with 32 V to the restricted mode occurs, the designated TE shall not lose an established call when the power source for the restricted mode provides an open circuit voltage of 40 V with a limited current of 11 mA. The TE shall be able to reach the steady state which allows the power source to leave the current limiting condition.

A designated and activated TE being in restricted mode and detecting transition to normal mode shall not change its power consumption limit (380 mW) to 1 Watt before 500 ms after detection of the reversed polarity.

7.1.4 Other power source requirements

7.1.4.1 Power source 1 restricted

The power source shall be able to increase the output voltage from 1 V to 34 V within 1,5 s, within 10 s after removal of a short circuit applied for up to 30 minutes, at its output with a test load of 100 µF connected to it.

7.1.4.2 Power source 1 normal

Two alternative power source implementations concerning overload and short-circuit protection were taken into account:

a) sources limiting the output current (fall back characteristic);

b) sources with switch off/switch on characteristic.

7.1.4.3 Requirements for type (a) sources

The power source shall be able to increase the output voltage from 1 V to 34 V within 350 ms, within 10 s after removal of a short circuit applied for up to 30 minutes, at its output with a test load of n times the TE equivalent (as defined in figure 4) connected to it (with the lowest acceptable voltage level at the mains interface of power source 1).

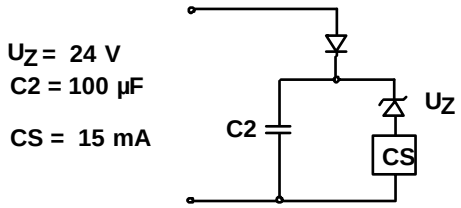


Figure 4: TE equivalent

7.1.4.4 Requirements for both types of sources

It should be noted that in the following subclauses the term n is used for the maximum number of terminals to be fed via the interface.

7.1.4.4.1 Switch-on surge capability

When switching power on to the interface, or after the change from restricted to normal condition, the PS1 shall provide a minimum current of n times 45 mA for at least 100 ms and the voltage shall be at least 30 V during this time period. After the time of 100 ms, the power source shall be able to provide the power of n times 1 Watt and the power drop on the interface with the output voltage within the specified limits.

7.1.4.4.2 TE connection surge capability

PS1 normal shall be able to provide, for at least 100 ms, an additional current of 50 mA when the constant current drawn from the source was (n-1) times 30 mA before this current surge and shall be n times 30 mA after it. The output voltage shall not drop below the minimum value of 34 V during the test. It should be noted that n is the maximum number of terminals to be fed via the interface.

7.2 Current unbalance

7.2.1 Direct current unbalance

The unbalanced maximum direct current flowing in the transformer windings can be caused by:

a) resistance unbalance of the transformer circuit of Nts;

b) resistance unbalance of the transformer circuit of TEs having power sink 1;

c) differential resistance in a pair of the installation wiring.

7.2.1.1 DC unbalance of PS1

The direct current unbalance (X) of the PS1 shall be less than 3 % of the current I (I1+I2) flowing through both phantom pairs when the maximum power provided by PS 1 is drawn.

Conformance shall be demonstrated with a test circuit as shown in figure 5 with resistors R (2 Ohm) to simulate a minimum equivalent of the TE cord and the installation.

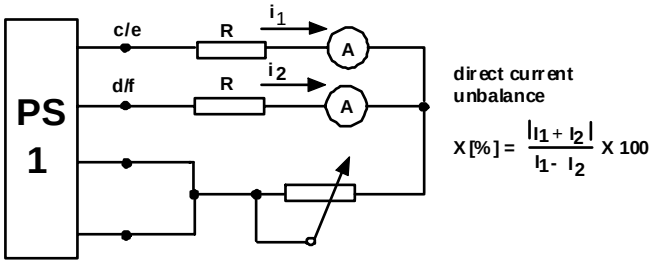


Figure 5: Test circuit for power source 1 DC unbalance measurement

7.2.1.2 DC unbalance of power sink 1

The direct current unbalance (X) of the power sink 1 shall be less than 3 % of the current I (I1+I2) flowing through both phantom pairs.

Conformance shall be demonstrated with a test circuit as shown in figure 6.

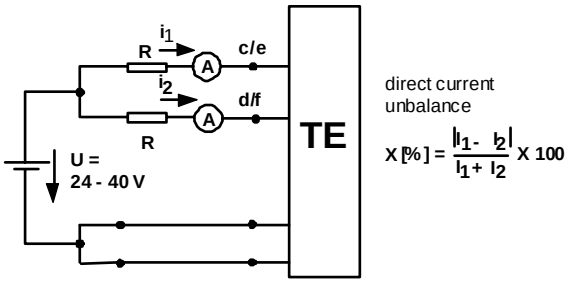


Figure 6: Test circuit for power sink 1 DC unbalance measurement

The resistors R (2 Ohm) represent the TE cord equivalent. When the TE under test is not provided with a cord, a cord having an ohmic resistance of at least 2 Ohm per conductor shall be used.

7.2.1.3 Differential resistance in a pair of the installation wiring

The difference of the ohmic resistance of the conductors of a pair shall be less than 3 % of the ohmic loop resistance of that pair, if the loop resistance is greater than 5 Ohm.

7.2.2 Current unbalance in a pair

A TE shall meet the specified electrical characteristics when an external current unbalance of X = 3 % is applied to its transformer.

Conformance shall be demonstrated with the test configuration as given in figure 7.

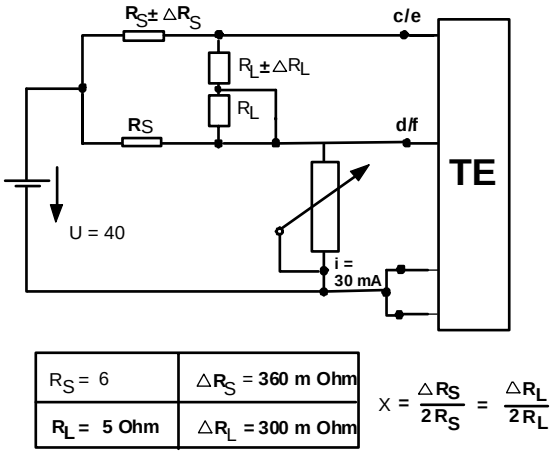


Figure 7: Test circuit for applied current unbalance

The impedance of the receiver and transmitter shall exceed the impedance indicated by the template in figure 12 of CCITT Recommendation I.430 [2] in the frequency range of 2 kHz to 20 kHz.

An NT shall meet the specified electrical characteristics as given in figure 11 of CCITT Recommendation I.430 [2] measured as defined in subclauses A.8.5.1.1 and A.8.6.1.2 in the frequency range of 2 kHz to 20 kHz, when an external DC unbalance of X = 3 % is adjusted and the maximum power provided by power source 1 is drawn.

NOTE: Wiring with different resistance unbalance (e.g. the use of existing wiring) may impose constraints on the application of the interface (i.e. limitation of the maximum number of Watts available from PS1 via the interface).

7.3 Additional requirements for an Auxiliary Power Supply (APS)

Unless stated otherwise, all PS1 requirements for the normal mode apply.

7.3.1 Power available for an APS

The APS shall support n terminals, where n is an integer number greater than or equal to 1. The APS shall provide an output power of 1 Watt for each terminal supported multiplied by a bus-wiring loading factor. The minimum loading factor is 1,1.

If the APS is to be capable of being connected at any interface point I_a on a short passive bus the required loading factor is at least 1,5. For a given loading factor the APS may support more terminals if connected in close proximity to the other terminals so that less power is consumed by the wiring.

7.3.2 APS switch-on time

When the APS switches power on to the interface (e.g. due to the application or restoration of its input power) or when first connected to the bus the voltage across the phantom at the APS output shall rise from 1 V to ≥ 34 V (but shall not exceed 42 V) within 2,5 ms and shall not fall below 34 V for a further period of 2,5 ms.

7.3.3 APS switch-off time

When the APS is no longer able to supply 34 V (for example when it no longer has its required input power) the voltage across the phantom at the APS output shall decay from 34 V to ≤ 1 V within 2,5 ms (and shall not rise above 1 V within a further 2,5 ms when tested in isolation from the NT1).

In the case where the APS has battery back-up, a considerable delay may occur between loss of input power to the APS and APS switch-off. In this case the provision of a battery low indication is an acceptable alternative.

7.3.4 APS power consumption when off

The APS shall not consume more than 3 mW from PS1 restricted mode when connected to the bus and the APS input power is not available.

7.3.5 Dynamic behaviour of APS

The same requirements as for PS1 normal located inside the NT1 also apply to an APS except that the APS shall meet the requirements for m = n + 1. The additional capability (equivalent to an additional terminal) allows for the support of n terminals plus the charge required to force the PS1 restricted mode to back-off.

7.4 Additional requirements for NT1 restricted mode source for compatibility with an APS

The NT1, designed to be compatible with an APS, shall not have a PS1 normal mode source.

Unless stated otherwise, all PS1 requirements for the restricted mode sources apply.

The APS can also be located inside the same physical equipment as a TE. In this case such a terminal shall not to be connected to a network that cannot support the APS (i.e. they do not have "Terminal Portability").

7.4.1 PS1 restricted mode back-off

The PS1 restricted mode source may have a detector to detect when the normal mode voltage appears on the phantom circuit and can switch-off the restricted mode source.

When a normal mode voltage appears at the interface point I_b the NT1 shall conform to the mask given in figure 2, with the values given in table 7, when tested in accordance with figure 1. In addition, a restricted mode load of 420 mW shall be connected to the NT1.

Table 7: Parameters for NT1 in restricted mode

A	5 µs	Y	45 mA
C	100 ms	X	current equivalent to 3 mW never exceeding 45 mA independent of the input voltage

7.4.2 PS1 restricted mode power-up

When the normal mode voltage at interface point I_b falls below 5 V, and before it falls to 2 V, the restricted mode source shall drive the phantom voltage into the restricted mode. The risetime from this voltage (2 V to 5 V) to ≤ - 34 V (but not below - 42 V) shall be < 2,5 ms. The PS1 voltage shall be in the range of - 34 V to - 42 V during the following 2,5 ms.

7.4.3 NT1 power consumption from APS normal mode

When the phantom voltage at interface point I_b is within the voltage range 24 V to 42 V the NT1 shall consume ≤ 3 mW.

Annex A (normative): Statements, modifications and additional requirements to CCITT Recommendation I.430 [2]

CCITT Recommendation I.430 [2] was written as a recommendation therefore the following table (table A.1: "Modifications and statements to CCITT Recommendation I.430 [2]") also gives an indication of the status of each requirement (i.e. normative, informative or not relevant).

Additional requirements to CCITT Recommendation I.430 [2] which are normative with respect to this ETS are provided in Clause 7 of this ETS.

Notes under normative Clauses/subclauses of I.430 [2] shall be considered as informative unless stated otherwise.

Definitions

N - normative: requirements with which it is necessary to comply in order to be able to claim compliance with this ETS. Therefore functions and features in clauses of CCITT Recommendation I.430 [2], stated as being normative in this ETS, shall be implemented and followed even if the text is given as a recommendation or example.

I - informative: the text of this Clause/subclause is provided for information. Titles for Clauses and subclauses are marked as informative when the requirements are given further subclauses.

N/R - not relevant: this Clause/subclause is not relevant to this ETS.

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2]

Clause/ subclause	Title <Comment>	St.- ment
	<See Scope of ETS 300 012>	
A.2	Service characteristics	I
A.2.1	Services required from the physical medium	I
A.2.2	Service provided to layer 2	I
A.2.2.1	Transmission capability	I
A.2.2.2	Activation/deactivation	I
A.2.2.3	D-channel access	I
A.2.2.4	Maintenance	I
A.2.2.5	Status indication	I
A.2.3	Primitives between layer 1 and the other entities	I
A.3	Modes of operation	I
A.3.1	Point-to-point operation	I
A.3.2	Point-to-multipoint operation	I
A.4	Types of wiring configuration	I
A.4.1	Point-to-point configuration	I
A.4.2	Point-to-multipoint configuration	I
A.4.3	Wiring polarity integrity	N
A.4.4	Location of the interfaces	N
A.4.5	NT and TE associated wiring	N
A.5	Functional characteristics	I
A.5.1	Interface functions	I
A.5.1.1	B-Channel	N
A.5.1.2	Bit timing	N
A.5.1.3	Octet timing	N
A.5.1.4	Frame alignment	N
A.5.1.5	D-Channel	N
A.5.1.6	D-Channel access procedure	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
A.5.1.7	Power feeding	N
	<The sentence in brackets "(In some applications unidirectional power feeding or no power feeding at all, across the interface, may apply) " is deleted>	
	<The term "NT" is replaced by "network side">	
	<The term "TEs" is replaced by "terminals">	
A.5.1.8	Deactivation	N
	<The sentence in brackets "(For some applications it will be appropriate for NTs to remain in the active state all the time)" is deleted>	
A.5.1.9	Activation	N
	<The sentence in brackets "(For some applications it will be appropriate for NTs to remain in the active state all the time)" is deleted>	
A.5.2	Interchange circuits	N
A.5.3	Connected/disconnected indication	I
A.5.3.1	TEs powered across the interface	N
A.5.3.2	TEs not powered across the interface	N
A.5.3.3	Indication of connection status	N
A.5.4	Frame structure	N
A.5.4.1	Bit rate	N
A.5.4.2	Binary organisation of the frame	N
	<NOTE 2 of figure 3/I.430 [2] is deleted>	
A.5.4.2.1	TE to NT	N
A.5.4.2.2	NT to TE	N
	<The NOTE under table 3/I.430 [2] is replaced by: "NOTE: S shall bet set to binary ZERO. Fa and M shall also be set to binary ZERO except for NT2 providing multiframing". This NOTE is normative.>	
	<The text to bit position 37 in table 3/I.430 [2] and under figure 3/I.430 [2]: "S - the use of this bit is for further study" is deleted; the following text is inserted: "S - reserved for future standardisation">	
A.5.4.2.3	Relative bit positions	N
A.5.5	Line code	N
A.5.6	Timing considerations	N
A.6	Interface procedures	I
A.6.1	D-Channel access procedure	I
A.6.1.1	Interframe (layer 2) time fill	N
A.6.1.2	D-echo channel	N
	<The text given in brackets under this clause is informative>	
A.6.1.3	D-Channel monitoring	N
A.6.1.4	Priority mechanism	N
A.6.1.5	Collision detection	N
A.6.1.6	Priority system	I
A.6.2	Activation/deactivation	I
A.6.2.1	Definitions	I
A.6.2.1.1	TE states	I

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
A.6.2.1.1.1	State F1 <The first sentence is replaced by: "STATE F1 (inactive): In this inactive (powered-off) state, the TE is not transmitting and cannot detect the presence of any input signals.">	N
A.6.2.1.1.2	State F2 <At the end of this subclause a sentence is added: "When in this state, a TE may go to a low-power consumption mode as specified in subclause A.5.1.8.">	N
A.6.2.1.1.3	State F3 <At the end of this subclause a sentence is added: "When in this state, a TE may go to a low-power consumption mode as specified in subclause A.5.1.8.">	N
A.6.2.1.1.4	State F4	N
A.6.2.1.1.5	State F5	N
A.6.2.1.1.6	State F6	N
A.6.2.1.1.7	State F7 is the only state where B and D channels contain operational data.	N
A.6.2.1.1.8	State F8	N
A.6.2.1.2	NT states	I
A.6.2.1.2.1	State G1	N
A.6.2.1.2.2	State G2 <The term "NT" in the last sentence is amended to "network side">	N
A.6.2.1.2.3	State G3	N
A.6.2.1.2.4	State G4	N
A.6.2.1.3	Activate primitives	N
A.6.2.1.4	Deactivate primitives	N
A.6.2.1.5	Management primitives	N
A.6.2.1.6	Valid primitive sequences	I
A.6.2.2	Signals <NOTE 1 of Table 4/I.430 [2] is normative, the word "should" in the second sentence is replaced by "shall"> <NOTE 3 of Table 4/I.430 [2] is replaced by: "NOTE 3 - For the transmission of INFO 0, the duration of a state in which the signal "consecutive binary ONEs" is transmitted is relevant rather than the definition of INFO 0 in terms of a time. The duration of a state depends on events (e.g. service primitives) and may be indefinitely short.">	N
A.6.2.3	Activation/deactivation procedure for TEs	I
A.6.2.3.1	General TE procedures	N
A.6.2.3.2	Specification of the procedure <Table 5/I.430 [2] shall be modified as follows: - under state F4 a state transition to F6 shall occur with NOTE 4 at the event "receive INFO 2". - under state F4 a state transition to F7 shall occur with NOTE 4 and PH-AI/MPH-AI primitives at the event "receive INFO 4". - "NOTE 4" shall be deleted under state F5 at the events "receive INFO 2" and "receive INFO 4".	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	- under state F6 the transition to F3 is deleted at the event "Expiry of timer T3" (the primitives are kept)> - under states F3, F4, F5, F6 and F8 timer T3 shall be stopped and reset at the event "Receive INFO 4"> - under state F7 the sign "-" is replaced by "/" at the event "Expiry of T3"> - under state F8 the sign "-" is replaced by MPH-DI, PH-DI, F3 at the event "expiry of T3". <"Annex C" is changed to read "Annex C/I.430"> <NOTEs 2 and 4 to table 5/I.430 [2] are normative> <In the last sentence of NOTE 2 the term "TE" is amended to "terminal"> <In the last sentence of NOTE 2 the term "NT" is amended to "network"> <The following text is added to NOTE 4 under table 5/I.430 [2]: "If INFO 2 or INFO 4 is not recognised within 5 ms after the appearance of a signal, TE shall go to F5. "To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronise, operation of TEs shall be verified where the received signal is any bit pattern (containing at least 3 ZEROs in each frame interval) to which TEs conforming to subclause A.6.3.1.2 are not able to synchronise."> <A new normative NOTE 5 is added to table 5/ I.430 [2] under the event "Rec, INFO 0": "NOTE 5 - INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in table 5/I.430 [2]. "Conformance shall be tested with a sinusoidal signal having a voltage of 100mV peak-to-peak (with a frequency in the range of 2kHz to 1000 kHz, preferably 100 kHz). "TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms."> <A new normative NOTE 6 is added to the event "Receiving INFO 0" in table 5/I.430 [2]: "NOTE 6 - A timer is started when leaving State F7 or F8 upon the reception of INFO 0. "The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter an active state before expiry of this timer. The value of this timer is in the range of 500 ms to 1000 ms. "This prevents the loss of an on-going communication caused by spurious effects.">	
A.6.2.4 A.6.2.4.1	Activation/deactivation for NTs Activating/deactivating NTs <The headline of this subclause is deleted, the text under this subclause is inserted under subclause 6.2.4>	I N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	<NOTE 2 to table 6/I.430 [2] is normative> <The fourth sentence of NOTE 2 is replaced by: "If the NT is able to unambiguously recognise INFO 1, then the value of Timer 2 may be 0, and an MPH-Deactivate Request would cause a direct transition from state G2 or G3 to G1. "It should be noted that unambiguous detection of INFO 1 may not be possible in passive bus configurations, considering all possible implementations."> <A new normative NOTE 5 is added to table 6/ I.430 [2] under the event "Rec, INFO 0": "NOTE 5 - INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the NT shall perform the actions specified in table 6/I.430 [2]. "For conformance test purposes, in the state G3 when receiving a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1000 kHz, preferably 100 kHz), the NT shall react by transmitting INFO 2 within a period of time 250 µs to 25 ms. "It is recognised that the action in state G4 cannot be observed or verified at the interface.">	
A.6.2.4.2	Non-activating/non-deactivating NTs	N/R
A.6.2.5	Timer values	N
A.6.2.6	Activation times	I
A.6.2.6.1	TE activation times <The text given in brackets under this subclause is informative> <In the first paragraph, the second sentence shall start with: "In state F6, ..."> <In the second paragraph the term "INFO 2" is replaced (three times) by: "INFO 2 or INFO 4">	N
A.6.2.6.2	NT activation times	N
A.6.2.7	Deactivation times	N
A.6.3	Frame alignment procedure	N
A.6.3.1	Frame alignment procedure in the direction NT to TE	N
A.6.3.1.1	Loss of frame alignment	N
A.6.3.1.2	Frame alignment	N
A.6.3.2	Frame alignment procedure in the direction TE to NT <The end of the sentence (and including) "except if the Q-channel..." is deleted>	N
A.6.3.2.1	Loss of frame alignment	N
A.6.3.2.2	Frame alignment	N
A.6.3.3	Multiframing <The complete text under 6.3.3/I.430 [2] is replaced by: "The multiframing mechanism is intended to provide extra layer 1 capacity in the TE-to-NT direction (Q channel). The use of multiframing is out of the scope of this ETS. The NT1 shall not provide multiframing, therefore the FA bit in the frame NT-to-TE (see figure 3/I.430 [2]) shall be set to binary ZERO. The NT2 may	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	The NT2 may provide multiframing in accordance with CCITT Recommendation I.430 [2], 6.3.3. "However, TEs shall provide for identification of the bit positions which provide this extra capacity, designated Q-bits. "The TE shall echo the binary value of the received FA bits in the corresponding FA bit position of the frame transmitted to the NT.">	
A.6.3.3.1	General mechanism	N/R
A.6.3.3.2	Q-bit position identification algorithm	N/R
A.6.3.3.3	TE multi-frame identification	N/R
A.6.3.4	S-bit channel structuring algorithm	N/R
A.6.4	Idle channel code on the B-channels	N
A.7	Layer 1 maintenance	I
A.8	Electrical characteristics	I
A.8.1	Bit rate	I
A.8.1.1	Nominal bitrate	N
A.8.1.2	Tolerance	N
A.8.2	Jitter and bit phase relationship between TE input and output	I
A.8.2.1	Test configurations	N
A.8.2.2	Timing extraction jitter	N
	<The first sentence is modified to read: "(3 dB point) of 30 Hz and an asymptotic roll off of 20 dB per decade under the ...">	
A.8.2.3	Total phase deviation input to output	N
A.8.3	NT jitter characteristics	N
A.8.4	Termination of the line	N
A.8.5	Transmitter output characteristics	I
A.8.5.1	Transmitter output impedance	N
A.8.5.1.1	NT transmitter output impedance	N
	<The beginning of the first sentence under a) is changed to read: "a) At all times except when transmitting a binary ZERO, ..."> <The term "at least" in the sentence "This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value)" is deleted.> <The NOTE under part b) is normative> <The first sentence of the NOTE under part b) is modified to read: "The output impedance limit shall apply for the 50 ohm nominal load condition.">	
A.8.5.1.2	TE transmitter output impedance	N
	<The beginning of the first sentence under a) is changed to read: "a) At all times except when transmitting a binary ZERO, ..."> <The term "at least" in the sentence "This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value)" is deleted.> <The NOTE is normative>	
A.8.5.2	Test load impedence	N
A.8.5.3	Pulse shape and amplitude (binary ZERO)	I
A.8.5.3.1	Pulse shape	N
A.8.5.3.2	Nominal pulse amplitude	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
A.8.5.4	Pulse unbalance <The text under this subclause is replaced by: "The unbalance may be the consequence of ICs tolerance or circuit design but also the consequence of the dynamic behaviour of the power feeding circuit of the transmitter which may result in a pattern dependent pulse amplitude."> <Two new normative subclauses are added:	N
A.8.5.4.1	"Pulse amplitude when transmitting a high density pattern "For both positive and negative pulses, 2 thresholds are set, corresponding to the minimum and maximum amplitude defined by the pulse mask (nominal amplitude +/-10 %). "When transmitting 40 frames with continuous binary ZERO in at least both B-channels into a test load of 50 Ohm the pulse amplitude in the middle of the pulse shall be within the threshold as given in figure 13/I.430 [2].	N
A.8.5.4.2	"Pulse unbalance of an isolated couple of pulses "The absolute sum of ^ U (t) dt for a positive pulse (one bit) and of ^ U (t) dt for a negative pulse (one bit) shall be < 5 % of the nominal pulse. Therefore the reference voltage is given by the signal when transmitting INFO 0. The edge between two adjacent pulses shall be the crossing of the zero voltage. From this edge the integral shall be defined for a time period of 1.5 UI in each direction. "For TEs the conformance test shall be performed with the first frame INFO 3 containing all binary ONEs in both B-channels and in the D-channel following INFO 0. "For NTs the conformance test shall be performed with the signal INFO 4. In the B1-channel two alternated octets 1111 1111 and 1111 1100 shall be inserted so that the two binary ZEROs are set in the bit position 33 and 34 (see table 3/I.430 [2]). All B2-, D- and E-bits shall be set to binary ONE.">	N
A.8.5.5 A.8.5.5.1 A.8.5.5.2	Voltage on other test loads (TE only) 400 Ohm load 5.6 Ohm load	N N N
A.8.5.6 A.8.5.6.1	Unbalance about earth Longitudinal conversion loss <The formula under a) is replaced by: "10 kHz ≤ f ≤ 300 kHz: ≥ 54 dB">	N N
A.8.5.6.2	Output signal balance <The output signal balance requirements are covered by prEN 50096 [6]>.	N/R
A.8.6 A.8.6.1	Receiver input characteristics Receiver input impedance	I I
A.8.6.1.1	TE receiver input impedance <The text under this subclause is replaced by:	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	"TEs shall meet the same input impedance requirements as specified in A.8.5.1.2 a), i and ii for the output impedance independently of the state of the terminal (F1 to F8).">	
A.8.6.1.2	NT receiver input impedance <The first sentence is replaced by: "At all times, the following requirements apply:"> <The term "at least" in the sentence "This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value)" is deleted.>	N
A.8.6.2	Receiver sensitivity - Noise and distortion immunity	N
A.8.6.2.1	TEs	N
A.8.6.2.2	NTs for short passive bus (fixed timing)	N
A.8.6.2.3	NTs for both point-to-point and short passive bus configurations (adaptive timing)	N
A.8.6.2.4	NTs for extended passive bus wiring configurations	N
A.8.6.2.5	NTs for point-to-point configurations only	N
A.8.6.3	NT receiver input delay characteristics	I
A.8.6.3.1	NT for short passive bus	N
A.8.6.3.2	NT for both point-to-point and passive bus	N
A.8.6.3.3	NT for extended passive bus	N
A.8.6.3.4	NT for point-to-point only	N
A.8.6.4	Unbalance about earth	N
A.8.7	Isolation from external voltages <These requirements are defined in prETS 300 047 [7]>	N/R
A.8.8	Interconnecting media characteristics <The text under this subclause is replaced by: "Interface cables (or cabling) shall include twisted metallic pairs (two to four as required). Such pairs are frequently part of the customers distribution systems. The transmission characteristics of the transmit and receive pairs shall be such that satisfactory operation is assured when used to interconnect (Ia to Ib) equipment having interfaces conforming to requirements of this ETS. Examples of cable systems parameters that must be considered are loss, frequency response, crosstalk loss, longitudinal balance and noise. NOTE: that cable characteristics assumed in defining the requirements specified in this ETS at interface point Ia and Ib are discussed in Annex A/I.430 [2] and in table D-1/I.430 [2]. Longitudinal balance, e.g. ± 43 dB at 96 kHz, is of particular importance to assure compliance with EMI limitations which must also be considered in determining suitable interface cables.">	N
A.8.9	Standard ISDN basic access TE cord <The sentence "- the resistance of an individual conductor shall not exceed 3 Ω." is replaced by: "- the resistance R of an individual conductor shall not exceed 3 Ω. The difference in the resistance of the conductors of a pair shall not exceed 60 mΩ + 0,04 R.">	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	<Under the fifth line of alinea a), the sentence is modified to read: "... at both ends in identical plugs ..."> <The second sign "-" is deleted under alinea b); the penultimate sentence starts at the left margin>	
A.9	Power feeding <A new sentence is inserted under this clause: "All the values referring to power in Watts shall be measured using an instrument which integrates the measurement over a period of 50 ms".> <NOTE: It should be noted that CCITT is currently discussing a second nominal voltage for power feeding with 48 V. Therefore terminals may need to operate in a voltage range between 24 and 56 V (see CCITT list of items to be studied for I.430 [2]).> <NOTE: According to CCITT I.430 [2] list of items to be studied the definition of power values provided by power sources or consumed by power sinks may be changed from fixed values to Power Consumption Units (PCU). This concept has not yet been adopted in this ETS. Further study is required especially on backward compatibility.>	N
A.9.1	Reference configuration <Additional notes to figure 20/I.430 [2]: NOTE 4: Power source 2 may also be implemented as a separate device and attached to the interface wiring outside of NT. NOTE 5: NT requiring remote power feeding from a TE via the interface shall implement a power sink. NOTE 6: In TE-to-TE application remote power feeding of a TE from an other TE may be performed by application of power source 3>	I
A.9.1.1 A.9.1.2	Functions specified at the access leads Provision of power sources and sinks <The text of subclause 9.1.2/I.430 [2] is replaced by the following text: "The provision of power source 1 (normal) is optional. NOTE: Optional in this case refers only to the responsibility of the network provider for the provision of power source 1. The capability of the provision of power source 1 shall always be available, either: as an integral part of the NT1, and/or; - physically separate and connected at any point in the interface wiring. "The provision of power source 1 (restricted) is mandatory.	N N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	NOTE: Mandatory in this case refers only to the responsibility of the network provider for the provision of power source 1 (restricted) in a single basic access configuration. In the case of a multiple basic access to an NT2 configuration, power source 1 (restricted) shall be mandatory for at least one of the NT1 accesses. "In some cases the provision of power source 1 (restricted) can be guaranteed only for a limited period of time. The provision of power source 2 is optional. The provision of power source 3 is outside the scope of this ETS." Power sinks 1 and 2 are optional>	
A.9.2	Power available from NT	N
A.9.2.1	Power source 1 normal and restricted power conditions <The reference to the note under subclause 9.3.1.1/I.430 [2] is deleted.>	N
A.9.2.2	Minimum voltage at NT from PS1	N
A.9.2.2.1	Normal power conditions	N
A.9.2.2.2	Restricted power conditions	N
A.9.2.3	Minimum voltage of PS2	N
A.9.3	Power available at TE	I
A.9.3.1	Power source 1 - phantom mode	I
A.9.3.1.1	Normal power conditions <The NOTE under this subclause is deleted>	N
A.9.3.1.2	Restricted power conditions	N
A.9.3.2	Power source 2 - optional third pair	I
A.9.3.2.1	Normal power conditions	N
A.9.3.2.2	Restricted power conditions	N
A.9.4	Current transient <The text under this subclause is replaced by: "The rate of change of current drawn by the TE shall not exceed 5 mA/µs. This requirement is not applicable during 100 ms or a time C according to figure 2 of this ETS as elapsed (see also Annex C) after the connection of the terminal.">> <NOTE: See subclause 7.1 of this ETS.>	N
A.9.5	Power source 1 consumption	N
A.9.5.1	Normal power conditions <NOTE: Permitted leakage current is defined in subclause 7.1.1 to this ETS.> <The reference to the note under subclause 9.3.1.1 is deleted.> <The end of the fourth sentence is modified to read: "..this TE shall enter a "local action" state">	N
A.9.5.2	Restricted power conditions	I
A.9.5.2.1	Power available to the TE "designated" for restricted power operation <In the second sentence the term "powered down" is replaced by "in low-power mode"> <The third sentence is replaced by:	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	"The value of the low-power mode consumption shall be ≤ 25 mW."> <The NOTE under this subclause is deleted> <NOTEs 1, 2 and 3 under table 8/I.430 [2] are deleted> <A new NOTE is added under both boxes indicating "0 mW": "NOTE - See subclause A.9.5.2.2">	
A.9.5.2.2	Power available to "non-designated" TEs <The complete text under this subclause is replaced by: "TEs not powered from power source 1 having a disconnection detector which utilises the phantom voltage shall not draw more than 3 mW from the interface. "TEs not powered from power source 1 not having a disconnection detector which utilises the phantom voltage and non-designated TEs which are normally powered from power source 1 (normal conditions) shall not consume any power from power source 1 in restricted power conditions."> <NOTE: Permitted leakage current is defined in subclause 7.1.1 to this ETS.>	N
A.9.6	Galvanic isolation <At the end of the text a new sentence is added: "See also ETS 300 047 [7]">	N
A.10	Interface connector contact assignments <The first sentence under this clause is replaced by: "The interface connector and the contact assignments are defined in prEN 28 877 [4] AND ENV 41 001 [5]."> <The NOTE to table 9/I.430 [2] is deleted>	N
A.Annex A	Wiring configurations and round trip delay considerations used as a basis for electrical characteristics	I
A.Annex B	SDL representation of a possible implementation of the D-channel access	I
A.Annex C	SDL representation of activation/deactivation procedures for TEs which can detect power source 1 or power source 2 <When SDL representation and activation/ deactivation tables are inconsistent, the tables shall apply> <Under state F6 at the event "Expiry of timer T3" the state "F3" in the final box is replaced by "F6"> <Under states F3, F4, F5, F6, and F8 timer T3 shall be stopped and reset at the event "receive INFO 4">	I

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
A.Annex C	Table C-1/I.430 [2] <The event "Application of power" is replaced by: "Power on and detection of power"> <The signs "/" at the event "Power on and detection of power" are replaced by the sign "-" under the states F2, F3, F4, F5, F6, F7 and F8.> <Under state F6 the transition to F3 is deleted at the event "Expiry of timer T3" (the primitives are kept)> <Under states F3, F4, F5, F6 and F8 timer T3 shall be stopped and reset at the event "Receive INFO 4"> <Under state F7 the sign "-" is replaced by "/" at the event "Expiry of T3"> <NOTE 3 to table C-1/I.430 [2] is normative> <Under state F8 the sign "-" is replaced by MPH -DI, PH-DI, F3 at the event "expiry of T3">. <The following text is added to NOTE 3 under table C-1/I.430 [2]: "If INFO 2 or INFO 4 is not recognised within 5 ms after the appearance of a signal, TE must go to F5. "To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronise, operation of TEs shall be verified where the received signal is any bit pattern (containing at least 3 ZEROs in each frame interval) to which TEs conforming to subclause A.6.3.1.2 are not able to synchronise."> <"(NOTE 2)" in the box "Receiving any signal" is changed to: "(NOTE 1)"> <A new normative NOTE 4 is added to the event "Receiving INFO 0" in table C-1/I.430 [2]: "NOTE 4 - A timer is started when leaving the states F7 or F8 upon the reception of INFO 0. "The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter an active state before expiry of this timer. "The value of this timer is in the range of 500 ms to 1000 ms. "This prevents the loss of an on-going communication caused by spurious effects."> <A new normative NOTE 5 is added to table C-1/ I.430 [2] under the event "Rec, INFO 0": "NOTE 5 - INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in table C-1/I.430 [2]. "Conformance shall be tested with a sinusoidal signal having a voltage of 100mV peak-to-peak (with a frequency in the range of 2kHz to 1000kHz, preferably 100 kHz).	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	"TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms.">	
A.Annex C	Table C-2/I.430 [2]	N
	<The event "Application of power" is replaced by: "Power on and detection of power">	
	<The signs "/" at the event "Power on and detection of power" are replaced by the sign "-" under the states F1.1, F2, F3, F4, F5, F6, F7 and F8.>	
	<Under state F6 the transition to F3 is deleted at the event "Expiry of timer T3" (the primitives are kept)>	
	<Under states F2, F3, F4, F5, F6 and F8 timer T3 shall be stopped and reset at the event "Receive INFO 4">	
	<Under state F7 the sign "-" is replaced by "/" at the event "Expiry of T3">	
	<under state F1.1 the sign "/" is replaced by "(NOTE 6)" at the events "receive INFO 2" and receive INFO ".>.	
	"<NOTE 6: Two possibilities exist for the reaction in these cases. case 1: MPH-II(c), MPH-AI, PH-AI, stop reset T3, F7; this reaction is appropriate when INFO 4 is detected to supplement the connection status. MPH-II(c), stop reset T3, F6; this reaction is appropriate when INFO 2 is detected to supplement the connection status. case 2: "/" (impossible); this reaction is to be applied when the connection status is determined by the presence or absence of power.>".	
	<Under states F6 and F7 at the event "Disappearance of power S" the indication of "MPH-II(d), MPH-DI, PH-DI; F1.1" is replaced by the sign: "-" (no state change)>	
	<Under states F6 and F7 at the event "Detect power S" the sign "/" is replaced by: "-" (no state change)>	
	<Under state F8, the sign "-" is replaced by MPH-DI, PH-DI, F3 at the event "expiry of T3".>	
	<NOTE 3 to table C-2/I.430 [2] is normative>	
	<The following text is added to NOTE 3 under table C-2/I.430 [2]: "If INFO 2 or INFO 4 is not recognised within 5ms after the appearance of a signal, TE must go to F5.	

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (continued)

Clause/ subclause	Title <Comment>	St.- ment
	"To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronise, operation of TEs shall be verified where the received signal is any bit pattern (containing at least 3 ZEROs in each frame interval) to which TEs conforming to subclause A.6.3.1.2 are not able to synchronise."> <A new normative NOTE 4 is added to the event "Receiving INFO 0" in table C-2/I.430 [2]: "NOTE 4 - A timer is started when leaving the states F7 or F8 upon the reception of INFO 0. "The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter an active state before expiry of this timer. "The value of this timer is in the range of 500 ms to 1000 ms. "This prevents the loss of an on-going communication caused by spurious effects."> <A new normative NOTE added to table C-2/ I.430 [2] under the event "Rec, INFO 0": "NOTE 5 - INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in table C-2/I.430 [2]. "Conformance shall be tested with a sinusoidal signal having a voltage of 100 mV peak-to-peak 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1000 kHz, preferably 100 kHz) "TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms.">	
A.Annex C	SDL representation of activation/deactivation procedures for NTS <In the SDL representation of the activation/ deactivation procedures for NTs the action "start timer 2" under state G4 is replaced by: "start timer 1">	I
A.Annex D	Test configurations	N
A.Annex E	Vocabulary of terms used in connection with Recommendations I.430 [2], I.431 [10], G.960 [11] and G.961 [12].	I
A.Appendix I	Test loopbacks defined for the basic user-network interface <The first sentence under subclause I.4/I.430 [2] is replaced by: "Table I-1 presents the characteristics applicable to each recommended loopback."> <The loopback 2 shall be implemented> <NOTE 4 under table I-1/I.430 [2] is normative> <Loopbacks C, B1, B2, A and NOTES 1, 2 and 3 are deleted from table I-2/I.430 [2]> <NOTE 4 is renumbered to NOTE 1>	N

Table A.1: Modifications and statements to CCITT Recommendation I.430 [2] (concluded)

Clause/ subclause	Title <Comment>	St.- ment
	<The following informative NOTE is added under table I-2/I.430 [2]: "NOTE 2: For conformance test purposes it is desirable that a complete loopback 4 as defined in table I-2/I.430 [2] is provided by an item under test. "The loop control mechanism is up to the manufacturer and will have to be declared to the test house.">\ <Table I-3/I.430 [2] is deleted>	

Annex B (normative): Additional requirements applicable to the (explicit) S reference point

B.1 Introduction

This annex applies to the interface at the explicit S reference point, i.e. at the interface between a terminal and the Private Telecommunication Network eXchange (PTNX), see figure B.1.

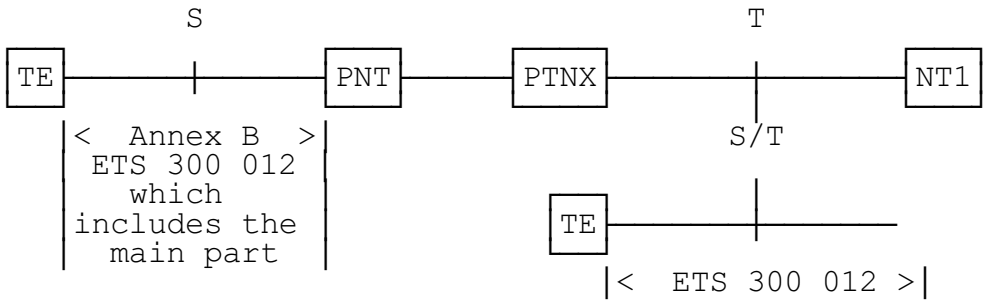


Figure B.1: Application of Annex B

B.2 References

CEN/CENELEC ENV 41 004 [8]: "Reference Configuration for Calls, based on ISDN Connection Types, as provided by Private Telecommunication Network Exchange"

B.3 Definitions

B.3.1 Private Network Termination (PNT)

A remote unit of equipment which terminates a transmission system employed between the private telecommunication network exchange and the interface I_b and the S reference point.

B.3.2 Terminal Equipment (TE)

The definition of the main body of this ETS applies with the exception that the NT2 functional grouping is not covered by this term within the context of this Annex.

B.4 Conformance

All normative statements of the main body of this ETS are subject to conformance with the understanding as indicated by Clause B.1 and subclauses B.3.1 and B.3.2.

B.5 Requirements

Multiframing (to be stated whether there shall be a difference to subclause A.6.3.3 as given in this ETS).

B.6 Provision of power

If reliable normal mode powering is provided by the PTNX to the interface the provision of restricted mode power is optional. The power source may have a connection to ground.

Annex C (informative): TE design to minimise power disturbance

To improve the performance of a TE for power transient conditions (connection, switch-on and switch- over between normal and restricted modes), consideration should be given to further limit the TE transient current within the mask given in subclause 7.1.1. By appropriate design of the TE, the transient current can be effectively eliminated, keeping its value below the steady-state current drawn by the TE.

For the first alternative the revised current/time mask is shown in figure C.1 for normal mode and in figure C.2 for restricted mode.

Other TE requirements would remain unchanged, except that the maximum effective capacitance limit should be reduced from 100 µF to 2 µF.

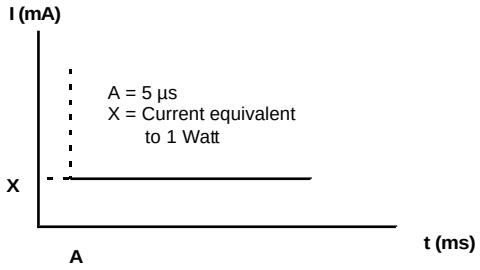


Figure C.1: Current/time limitation for TE in normal mode

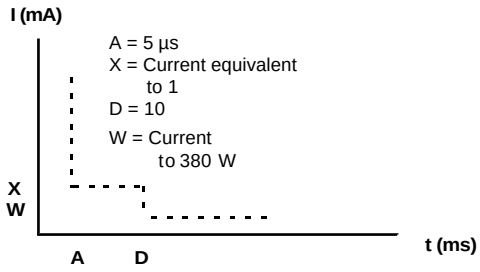
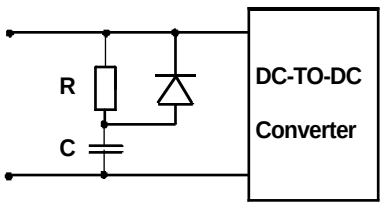


Figure C.2: Current/time limitation for TE in restricted mode

NOTE 1: The 2 µF limit is for capacitance measured directly at the PS1 input to the TE.

NOTE 2: Additional capacitance required to meet the holdover requirements has to be implemented so that it can still provide power for the DC-to-DC converter when needed. A possible implementation is suggested in figure C.3.



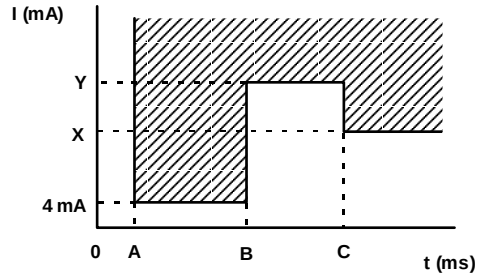
R = charging resistor
C = charging capacitor.

Figure C.3: TE holdover capacity

The TE discussed above will be fully capable of interworking with the power source as described in subclause 7.1.4. TEs meeting either specified limit can therefore be mixed within the same network and will provide basic functionality.

Furthermore, if all TEs connected to a given NT1 comply with the limits given in this Annex, then all TEs will potentially offer improved functionality during transient conditions. In addition, some of the power source requirements listed in subclause 7.1.4 can be simplified although in this case the power source may reduce interworking capability with terminals following the template given in subclause 7.1.1. Exact details of the revised power source requirements are for further study.

For the second alternative the revised current/time mask is shown in figure C.4.



A = 5 µs
5 µs ≤ B ≤ 900 ms
C = B + 100 ms
X, Y: see tables 2 and 3 of this ETS.

Figure C.4: Alternative current/time limitation for TEs

The current drawn should conform to the mask given in figure C.4.

In this case the current consumption during the waiting period (time between A and B) is limited to 4 mA. The maximum time between A and C is 1 s.

Annex D (normative): Conformance test principles to Interface Point I_a

D.1 Scope and general information

D.1.1 Scope

This annex provides the test principles for the requirements of this ETS used to determine the compliance of an Item Under Test to this ETS.

It is outside the scope of this annex to identify the specific tests required by an implementation where equipment has to meet attachment approval.

Detailed test equipment accuracy and the specific tolerance of the test devices is not a subject of this annex.

In the case where a PTNX does not use a connection cord at the T reference point, the location of interface I_a shall be declared by the PTNX supplier.

However, TEs using detachable connecting cords and designated for connection with a "standard ISDN basic access cord" shall meet the specified electrical characteristics in both cases as follows :

a) with the specific cord *(if any)* provided with the IUT;

b) with a reference cord conforming to the following requirements.

Parameter	C	Z	CL	R	D	L
Value	350 pF	> 75 Ω	> 60 dB	3 Ω	< 0,5 %	depends on the other parameters (see NOTE)
Tolerance	+ 0 %, - 10 %	-	-	+ 0 %,- 10 %	-	
NOTE: The total length of the cord depends on the parameters shown above. Nevertheless, this length should preferably by equal to 7 m and in any case shall be less than 10 m.						

C: capacitance of pairs for transmit and receive functions;
Z: characteristic impedance of pairs used for transmit and receive functions at 96 KHz;
CL: crosstalk loss at 96 kHz between any pair and a pair to be used for transmit or receive functions with terminations of 100 ohms ;
R: resistance of an individual conductor ;
D: difference of the ohmic resistance in each pair used for transmit and receive functions *(percentage of the ohmic loop resistance).*
L: length of the cord.

Detailed test equipment accuracy and the specification tolerance of the test devices is not a subject of this annex. Where such details are provided then those test details shall be considered as being an "informative" addition to the test description.

The test configurations given do not imply a specific realisation of test equipment or arrangement or the use of specific test devices for conformance testing. However, any test configuration used shall provide those test conditions specified under "system state", "stimulus" and "monitor" for each individual test *(the measurement arrangements and the equipment suggested are only for example purposes).*

Unless otherwise stated, conformance tests described in the present document do not apply to the Auxiliary Power Supply *(APS).*

D.1.2 General information

This document is applicable to interface I_a. The field of applicability is reported at the beginning of each test.

In the case of a multi-access item under test supporting interface I_a, unless otherwise stated, only one access at a time shall receive the stimulus. All other accesses shall receive "no signal".

For conformance test purposes, it is desirable that a complete loopback 4 is provided by an *IUT (see Annex A, Appendix I*) and also a test pattern of INFO 3 frames with the B1 and B2 channels set to binary ZERO.

IUT suppliers shall provide information on how IUT primitive exchanges can be detected i.e. primitives activate, deactivate, management primitives between layer 1 and higher layers.

Ideal values for components and circuits are considered in the test principles.

Unless otherwise stated the line termination resistors for both NT and TE side are considered inside the test equipment.

D.1.3 Definitions and abbreviations

For the purpose of this annex the following definitions and abbreviations, together with those given in Clause 3, apply :

IUT: Item Under Test. Interface point I_a, i.e. TE1, TA, NT2.

Rx: Receiver. Interface signal receiver of IUT or simulator.

Tx: Transmitter. Interface signal transmitter of IUT or simulator.

Simulator: Device generating the stimulus signal for the IUT and monitoring the signal transmitted by the IUT to find the result.

D.1.4 Allocation of tests

D.1.4.1 General

General	Clause / subclause	Test defined in Clause/subclause
General	A.1	N/R 1)

1) N/R: not relevant

D.1.4.2 Service characteristics

Services	Clause / subclause	Test defined in Clause/subclause
Service characteristics	A.2	N/R
Services required	A.2.1	N/R
Services to Layer 2	A.2.2	N/R
Transmission capability	A.2.2.1	N/R
act/deact	A.2.2.2	N/R
D-channel access	A.2.2.3	N/R
Maintenance	A.2.2.4	N/R
status indication	A.2.2.5	N/R
primitive	A.2.3	N/R

D.1.4.3 Modes of operation

Modes	Clause / subclause	Test defined in Clause/subclause
Modes of operation	A.3	N/R
Point to point	A.3.1	N/R
Point to Multipoint	A.3.2	N/R

D.1.4.4 Wiring

Modes	Clause / subclause	Test defined in Clause/subclause
Types of wiring configuration	A.4	N/R
Point-to-point configuration	A.4.1	N/R
Point-to-multipoint config.	A.4.2	N/R
Polarity Integrity (figure 2-I.430) [2]	A.4.3	N/R
Interface Ia	A.4.4	N/R
TE associated wiring	A.4.5	N/R

D.1.4.5 Functional characteristics

Functions	Clause / subclause	Test defined in Clause/subclause
Functional characteristics	A.5	N/R
Interface functions	A.5.1	N/R
B-channel	A.5.1.1	D.2.1.1
Bit timing	A.5.1.2	D.2.1.1
Octet timing	A.5.1.3	D.2.1.1
Frame alignment	A.5.1.4	D.3.3
D-channel	A.5.1.5	D.3.1.2
D-channel access procedure	A.5.1.6	D.3.1.2
Power feeding	A.5.1.7	D.5
Deactivation	A.5.1.8	D.3.2
Activation	A.5.1.9	D.3.2
Interchange circuits	A.5.2	D.2.1.1
Connect/disconnect indication	A.5.3	D.3.2
TE powered across interface	A.5.3.1	D.3.2
TE not powered across interface	A.5.3.2	D.3.2
Indication of connection status	A.5.3.3	D.3.2
Frame structure	A.5.4	D.2.1.1
Bit rate	A.5.4.1	D.2.1.1
Binary organisation of the frame	A.5.4.2	N/R
TE to NT	A.5.4.2.1	D.2.1.1
NT to TE	A.5.4.2.2	N/R
Relative bit positions	A.5.4.2.3	D.2.1.1
Line Code	A.5.5	D.2.1.1
Timing considerations	A.5.6	D.2.1.1

D.1.4.6 Interface procedures

Procedure = D-channel Access	Clause / subclause	Test defined in Clause/subclause
Interface procedures	A.6	N/R
D-channel Access procedure	A.6.1	N/R
Interframe (Layer 2) timefill	A.6.1.1	D.3.1.1
D-echo channel	A.6.1.2	N/R
D-channel monitoring	A.6.1.3	D.3.1.2
Priority mechanisms	A.6.1.4	D.3.1.2
Collision detection	A.6.1.5	D.3.1.2
Priority system	A.6.1.6	D.3.1.2
Activation/Deactivation	**Clause / subclause**	**Test defined in Clause/subclause**
Activation/Deactivation	A.6	N/R
Definitions	A.6.2.1	N/R
TE states	A.6.2.1.1	N/R
F1	A.6.2.1.1.1	D.3.2.1
F2	A.6.2.1.1.2	D.3.2.1
F3	A.6.2.1.1.3	D.3.2.1
F4	A.6.2.1.1.4	D.3.2.1
F5	A.6.2.1.1.5	D.3.2.1
F6	A.6.2.1.1.6	D.3.2.1
F7	A.6.2.1.1.7	D.3.2.1
F8	A.6.2.1.1.8	D.3.2.1
NT states	A.6.2.1.2	N/R
G1	A.6.2.1.2.1	N/R
G2	A.6.2.1.2.2	N/R
G3	A.6.2.1.2.3	N/R
G4	A.6.2.1.2.4	N/R
Activate primitives	A.6.2.1.3	D.3.2
Deactivation primitives	A.6.2.1.4	D.3.2
Management primitives	A.6.2.1.5	D.3.2
Valid primitive sequences	A.6.2.1.6	N/R
Signals	A.6.2.2	D.2.1.1, D.2.1.2
TE activation procedures	A.6.2.3	N/R
General TE procedures	A.6.2.3.1	D.3.2.1
Specification of procedure	A.6.2.3.2	D.3.2.1, D.3.2.2.6
Act/Deactivation on network side	A.6.2.4	N/R
Activating/Deactivating NT	A.6.2.4.1	N/R
Timer values	A.6.2.5	D.3.2.2.4
Activation time	A.6.2.6	N/R
TE activation times	A.6.2.6.1	D.3.2.2.1.1, D.3.2.2.1.2 D.3.2.2.2.1, D.3.2.2.2.2 D.3.2.2.3
NT activation times	A.6.2.6.2	N/R
Deactivation time	A.6.2.7	D.3.2.2.5

Procedure = Frame Alignment	Clause / subclause	Test defined in Clause/subclause
Frame alignment procedures	A.6.3	D.3.3
Frame alignment NT to TE	A.6.3.1	D.2.1.1, D.3.3
Loss of frame alignment	A.6.3.1.1	D.3.3
Frame alignment	A.6.3.1.2	D.3.3
Frame alignment TE to NT	A.6.3.2	N/R
Loss of frame alignment	A.6.3.2.1	N/R
Frame alignment	A.6.3.2.2	N/R
Multiframing	A.6.3.3	D.3.4
B-channel idle code	A.6.4	D.3.5

D.1.4.7 Maintenance

Functions	Clause / subclause	Test defined in Clause/subclause
Layer 1 maintenance	A.7	N/R

D.1.4.8 Electrical characteristics

Functions	Clause / subclause	Test defined in Clause/subclause
Electrical characteristics	A.8	N/R
Bit rate	A.8.1	N/R
Nominal bit rate	A.8.1.1	D.4.1
Tolerance	A.8.1.2	D.4.1
Jitter & bit phase	A.8.2	N/R
Test configurations	A.8.2.1	D.4.2.1, D.4.8.2
Timing extraction jitter	A.8.2.2	D.4.2.1
Total phase deviation	A.8.2.3	D.4.2.2
NT jitter characteristics	A.8.3	N/R
Termination of the line	A.8.4	N/R
Transmitter O/P characteristics	A.8.5	N/R
Transmitter output impedance	A.8.5.1	N/R
NT Transmitter output impedance	A.8.5.1.1	N/R
TE Transmitter output impedance	A.8.5.1.2	D.4.3
Test load impedance	A.8.5.2	N/R
Pulse shape and amplitude	A.8.5.3	D.4.4
Pulse shape	A.8.5.3.1	D.4.4
Nominal pulse amplitude	A.8.5.3.2	D.4.4
Pulse unbalance	A.8.5.4	N/R
- pulse amplitude (high density pattern)	A.8.5.4.1	D.4.5.1
- pulse unbalance of an isolated couple of pulses	A.8.5.4.2	D.4.5.2
Voltage on other test loads	A.8.5.5	D.4.6
400 ohm load	A.8.5.5.1	D.4.6.1
5.6 ohm load	A.8.5.5.2	D.4.6.2
Unbalance about earth	A.8.5.6	D.4.7
Longitudinal conversion loss	A.8.5.6.1	D.4.7
Output signal balance	A.8.5.6.2	N/R
Receiver Input Characteristics	A.8.6	N/R
Receiver Input Impedance	A.8.6.1	N/R
TE receiver input impedance	A.8.6.1.1	D.4.8.1
NT receiver input impedance	A.8.6.1.2	N/R
Receiver sensitivity (N & DI)	A.8.6.2	D.4.8.2
TEs	A.8.6.2.1	D.4.8.2
NTs for short passive bus	A.8.6.2.2	N/R
NT for pt-pt and short passive	A.8.6.2.3	N/R
NT for extended passive bus	A.8.6.2.4	N/R
NT for pt-pt only	A.8.6.2.5	N/R
NT receiver input delay	A.8.6.3	N/R
NT for short passive bus	A.8.6.3.1	N/R
NT for pt-pt and passive bus	A.8.6.3.2	N/R
NT for extended passive bus	A.8.6.3.3	N/R
NT for pt-pt only	A.8.6.3.4	N/R
Unbalance about earth	A.8.6.4	D.4.8.3
Isolation from external voltages	A.8.7	N/R
Interconnect media LCL	A.8.8	N/R
ISDN basic access TE cord	A.8.9	D.1.1

D.1.4.9 Power feeding

Static requirements	Clause / subclause	Test defined in Clause/subclause
Power Feeding	A.9	N/R
Reference configuration	A.9.1	N/R
Functions at the access leads	A.9.1.1	D.2.1.1, D.5.1.1.1
Provision of source and sinks	A.9.1.2	N/R
Power available from NT	A.9.2	N/R
PS1, normal and restricted	A.9.2.1	N/R
Min volts at NT from PS1	A.9.2.2	N/R
Normal condition	A.9.2.2. 1	N/R
Restricted power condition	A.9.2.2. 2	N/R
Min volts of power source 2	A.9.2.3	N/R
Power available at TE	A.9.3	N/R
Source 1 - phantom mode	A.9.3.1	N/R
Normal condition	A.9.3.1.1	D.5.1.1, D.5.1.4.4.2
Restricted power condition	A.9.3.1.2	D.5.1.2
Source 2 - optional pair	A.9.3.2	N/R
Normal condition	A.9.3.2.1	D.5.2
Restricted power condition	A.9.3.2.2	D.5.2
Current transient	A.9.4	D.5.1.3
Power source 1 consumption	A.9.5	N/R
Normal condition	A.9.5.1	D.5.1.1.1, D.5.1.1.2 D.5.1.1.3, D.5.1.1.4 D.5.1.1.5
Restricted power condition	A.9.5.2	D.5.1.2
Power available to designated TE	A.9.5.2.1	D.5.1.2 D.5.1.2.3
Power to non-designated TEs	A.9.5.2.2	D.5.1.2.4, D.5.1.2.5 D.5.1.2.6
Galvanic Isolation	A.9.6	N/R

Dynamic requirements	Clause / subclause	Test defined in Clause/subclause
Additional requirements	7	N/R
Limitations on power source and sink during transient conditions	7.1	D.5.1.4
Current/time limitations for TEs	7.1.1	D.5.1.4.1, D.5.1.4.2 D.5.1.4.3
Power source switch-over	7.1.2	N/R
Power source switch-over time	7.1.2.1	N/R
Restricted mode power source requirements under overload conditions	7.1.2.2	N/R
Other TE requirements	7.1.3	N/R
Minimum TE start-up current	7.1.3.1	D.5.1.4.4
Protection against short term interruptions	7.1.3.2	D.5.1.4.5
Behaviour at the switch-over	7.1.3.3	D.5.1.4.6
Effective capacitance at the PS1 input	7.1.3.4	N/R
Other power source requirements	7.1.4	N/R
Power Source 1 restricted	7.1.4.1	N/R
Power Source 1 normal	7.1.4.2	N/R
Requirements for type a) sources	7.1.4.3	N/R
Requirements for both types of sources	7.1.4.4	N/R
Switch-on surge capability	7.1.4.4.1	N/R
TE connection surge capability	7.1.4.4.2	N/R
Current unbalance	7.2	N/R
Direct current unbalance	7.2.1	N/R
DC unbalance of Power Source 1	7.2.1.1	N/R
DC unbalance of Power Sink 1	7.2.1.2	D.5.1.4.7
Differential resistance in a pair of the installation wiring	7.2.1.3	N/R
Current unbalance in a pair	7.2.2	D.5.1.4.8

Requirements from an APS	Clause / subclause	Test defined in Clause/subclause
Additional requirements	7.3	N/R
Power available from an APS	7.3.1	N/R
APS switch-on time	7.3.2	N/R
APS switch-off time	7.3.3	N/R
APS power consumption when off	7.3.4	D.5.1.1.4, D.5.1.4
Dynamic behaviour of APS	7.3.5	N/R
Additional requirements for NT1 restricted mode source for compatibility with an APS	7.4	N/R
PS1 restricted mode back-off	7.4.1	N/R
PS1 restricted mode power up	7.4.2	N/R
NT1 power consumption from APS normal mode	7.4.3	N/R

D.1.4.10 Interface connector and contact assignments

Requirements	Clause / subclause	Test defined in Clause/subclause
Reference configuration of leads	A.9.1.1	D.2.1.1, D.5.1.1.1
Contact assignments	A.10	D.2.1.1, D.5.1.1.1

D.1.4.11 Annexes

Requirements	Clause / subclause	Test defined in Clause/subclause
Test loopbacks defined for the basic user-network interface	Annex A App. I	N/R
Additional requirements applicable to the explicit S reference point	Annex B	N/R
TE design to minimise power disturbance	Annex C	N/R

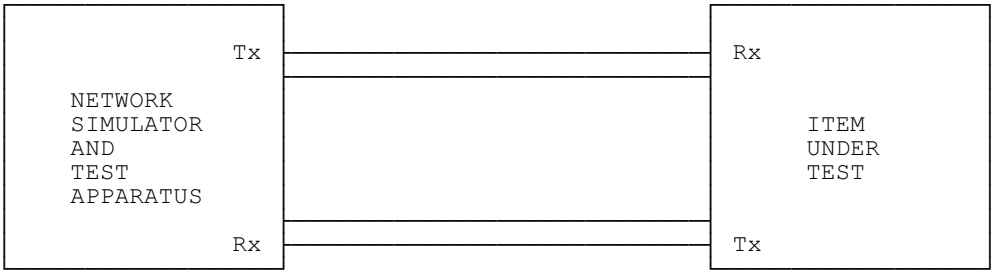
D.2 Functional characteristic tests (Clause A.5, ETS 300 012)

D.2.1 Binary organisation of frame

D.2.1.1 Test A (subclauses A.5.4.2.1, A.5.5, A.5.6, ETS 300 012)

Purpose: To check the binary organisation of INFO 3 frames.

Test configuration :



System state: Activated by the network simulator *(state F7)*. IUT transmitting a pseudo-random data pattern *(word length* ≤ 2^9-1) in the B-channels and idle channel code or messages in the D-channel.

Stimulus: INFO 4 type frames from the NT simulator. Fa bit set to ZERO

NOTE: If the IUT does not provide a loopback, an access to the B-channel of the IUT must be used for sending pseudo-random pattern *(see Clause D.1).*

Monitor : The frame structure from the TE (positive pulses, negative pulses and bit and frame timing are available).

Results:

BIT POSITION	DESCRIPTION	POLARITY
1	F-bit	positive pulse
2	L-bit	negative pulse
3-10	B1 octet	first binary ZERO coded negative, the following bits may be positive, negative or no pulse
11	L-bit	positive or no pulse
12	D-bit	negative or no pulse
13	L-bit	positive or no pulse
14	Fa	negative pulse
15	L-bit	positive pulse
16-23	B2 octet	first binary ZERO coded negative, the following bits may be positive, negative or no pulse
24	L-bit	positive or no pulse
25	D-bit	negative or no pulse
26	L-bit	positive or no pulse
27-34	B1 octet	first binary ZERO coded negative, the following bits may be positive, negative or no pulse
35	L-bit	positive or no pulse
36	D-bit	negative or no pulse
37	L-bit	positive or no pulse
38-45	B2 octet	first binary ZERO coded negative, the following bits may be positive, negative or no pulse
46	L-bit	positive or no pulse
47	D-bit	negative or no pulse
48	L-bit	positive or no pulse

NOTE 1: L = balance bit which is used to ensure even parity of data fields.

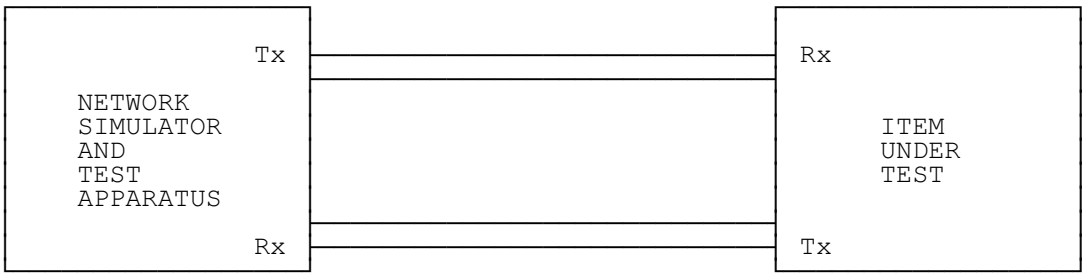
NOTE 2: See figure 3/I.430 [2] for details of pulse polarity.

NOTE 3: Multiframing procedure is not covered by this test.

D.2.1.2 Test B (subclause A.6.2.2, ETS 300 012)

Purpose: To check the binary organisation of INFO 1 frames.

Test configuration:



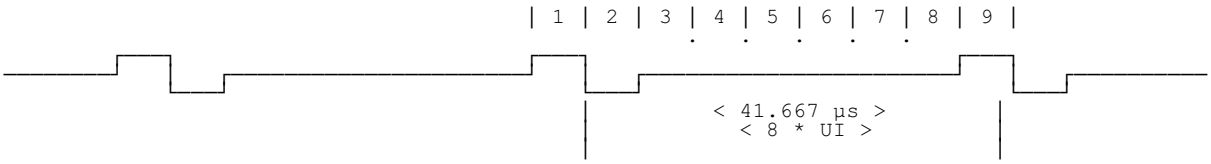
System state: Awaiting signal *(state F4)*.

Stimulus: Activation request from the IUT *(PH-AR)*.

Monitor: Line signals.

Results:

Check that the 8 bit pattern is contiguous and of the appropriate polarity.



D.3 Interface procedure tests (Clause A.6, ETS 300 012)

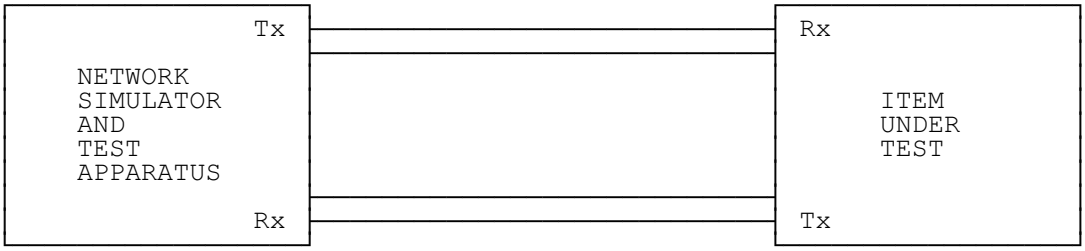
These tests are designed to test conformance to the specification of the interface procedures. The tests are performed by stimulating and monitoring the TE from the I.430 [2] bus and from activation requests of the user.

D.3.1 D-channel access control procedure (subclause A.6.1, ETS 300 012)

D.3.1.1 Interframe (layer 2) time fill (subclause A.6.1.1, ETS 300 012)

Purpose: To check the D-channel contains the correct interframe time fill from the TE.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: Interframe time fill on the D-channel.

Monitor: D-channel at the monitor port of the network simulator.

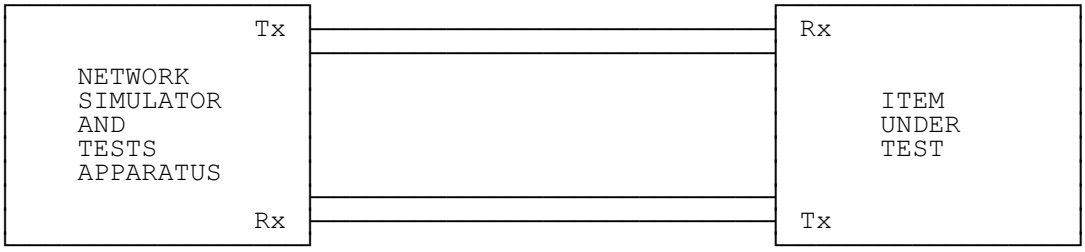
Results: Binary ONEs.

D.3.1.2 D-echo channel response (subclauses A.6.1.3 to A.6.1.6, ETS 300 012)

Purpose: To check if the TE detects collisions on the D-channel when transmitting, by means of the D-echo channel and ceases transmission immediately.

To check if the TE changes the priority level correctly within its priority class.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: D-channel data from the terminal side corrupted and returned in the D-echo channel.

Monitor: D-channel from the TE.

Results:

Result to Test *(a)* "MISMATCH"

Ensure that when the TE receives a binary ONE instead of a binary ZERO *(network error)* or a binary ZERO instead of a binary ONE *(collision)*, the TE detects the mismatch and ceases transmission immediately, i.e. the next D-bit received from the TE following the application of the stimulus is set to the idle condition *(Binary 1)*. This shall be ensured in each priority class and level which apply to the TE *(NOTE)*.

NOTE: The value of subsequent bits is related to priority class and priority level within the class and is covered by tests *(b)* and *(c)*.

The test shall be performed with binary ONE and binary ZERO.

Result to Test *(b)* "PRIORITY CLASS"

Ensure that after receipt by the TE of an errored D-echo channel bit, the TE while at the normal priority level receives at least 8 *(for Priority Class 1)* or at least 10 *(for Priority Class 2)*, according to the priority class of the Layer 2 frame to be transmitted, contiguous D-echo channel bits set to Binary ONE before transmission recommences.

Result to Test *(c)* "PRIORITY LEVEL"

Ensure that after successful transmission of a Layer 2 frame, the TE does:

- not commence the transmission of a subsequent Layer 2 frame until after the receipt of at least 9 *(for priority Class 1)* or at least 11 *(for Priority Class 2)* contiguous D-echo channel bits set to Binary ONE;

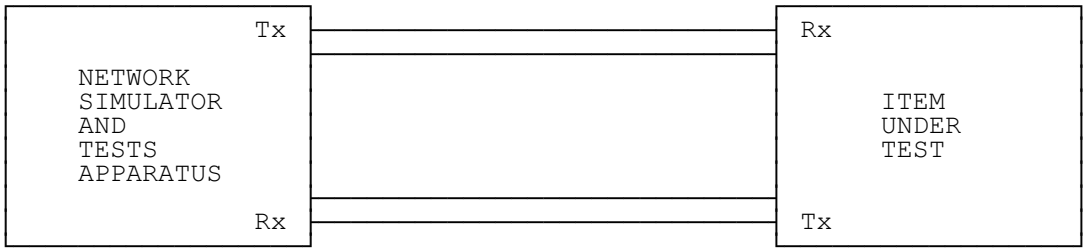
- change back to normal priority level after the receipt of 9 *(for Priority Class 1)* or 11 *(for Priority Class 2)* contiguous D-echo channel bits set to Binary ONE if no frame is available to be transmitted.

D.3.2 Activation/deactivation (subclause A.6.2, ETS 300 012)

D.3.2.1 Activation/deactivation procedure (subclause A.6.2, ETS 300 012)

Purpose: To check the terminal correctly executes the activation/deactivation procedure.

Test configuration:



System state: Any state.

Stimulus: Power supply 1 connected and disconnected, Line Signals INFOs 0, 2, 4 and any signal applied from the network and activation request *(PH-AR)* from the IUT.

NOTE: Multiframing procedure is not covered by this test.

Monitor: Line Signals : INFO 0, 1 and 3 at the network simulator.

Results : New state, transmitted signal (as described in the table below), and primitives sent to the higher layers according to table 5/CCITT Recommendation I.430 [2], table C.1/I.430 [2] or table C.2/I.430 [2].

STATE NO	CURRENT STATE	STIMULUS	NOTE	NEXT STATE	INFO SENT	COMMENT
1	F1	Power	1	F2	I0	Detection of power
2	F1	T3 expires	2/6	F1	I0	No action
3	F2	Loss of Power		F1	I0	Return to inactive state
4	F2	Rx INFO 0	4	F3	I0	Assume deactivated state
5	F2	Rx INFO 2		F6	I3	Synchronised state
6	F2	Rx INFO 4		F7	I3	Activated
7	F2	Rx any signal	3	F2	I0	No action
8	F2	T3 expires	6	F2	I0	No action
9	F3	Loss of Power		F1	I0	Return to inactive
10	F3	PH-AR		F4	I1	Initiate activation & T3
11	F3	Rx INFO 0	4	F3	I0	No action
12	F3	Rx INFO 2		F6	I3	Synchronised state
13	F3	Rx INFO 4		F7	I3	Activated
14	F3	Rx any signal	3	F3	I0	No action
15	F3	T3 expires	2	F3	I0	No action
16	F4	Loss of Power		F1	I0	Return to inactive state
17	F4	Rx INFO 0	4	F4	I1	No action
18	F4	Rx INFO 2	7	F6	I3	Synchronised
19	F4	Rx INFO 4	7	F7	I3	Active
20	F4	Rx any signal	3	F5	I0	Detection of signal
21	F4	T3 Expires	2	F3	I0	Deactivated
22	F5	Loss of Power		F1	I0	Return to inactive
23	F5	Rx INFO 0	4	F5	I0	No action
24	F5	Rx INFO 2		F6	I3	Synchronised
25	F5	Rx INFO 4		F7	I3	Activated
26	F5	Rx any signal	3	F5	I0	No action
27	F5	T3 Expires	2	F3	I0	Deactivated
28	F6	Loss of Power	8	F1	I0	Return to inactive
29	F6	Lost Framing		F8	I0	Loss of framing signals
30	F6	PH-AR		F6	I3	No action
31	F6	Rx INFO 0	4	F3	I0	Deactivated
32	F6	Rx INFO 2		F6	I3	No action
33	F6	Rx INFO 4		F7	I3	Activated
34	F6	T3 Expires	2	F6	I3	Synchronised
35	F7	Loss of Power	8	F1	I0	Return to inactive
36	F7	Lost Framing		F8	I0	Loss of framing
37	F7	Rx INFO 0	4/5	F3	I0	Deactivated
38	F7	Rx INFO 2		F6	I3	Synchronised
39	F7	Rx INFO 4		F7	I3	No action
40	F8	Loss of Power		F1	I0	Return to inactive
41	F8	PH-AR		F8	I0	No action
42	F8	Rx INFO 0	4/5	F3	I0	Deactivation
43	F8	Rx INFO 2		F6	I3	Synchronised
44	F8	Rx INFO 4		F7	I3	Activated
45	F8	Rx any signal	3	F8	I0	No action
46	F8	T3 expires	2	F8	I0	No action

NOTE 1: Because the IUT can be powered in different ways, it is useful to test this IUT with the possible power it is able to detect (PS1, PS2, local power).

NOTE 2: T3 = Implementation dependent, not to exceed 30 sec.

NOTE 3: "Any signal" is simulated by any bit pattern on which the IUT conforming to subclause A.6.3.1.2, ETS 300 012 is not able to synchronise.

NOTE 4: For testing purposes INFO 0 is simulated by a sinusoidal signal having a voltage of 100 mV peak to peak (with a frequency in the range of 2 kHz to 1000 kHz). The TE shall react by transmitting INFO 0 within a period time 250 µs to 25 ms.

NOTE 5: The PH-DI corresponding to the reception of INFO 0 shall be delivered to Layer 2 only if Layer 1 does not re-enter an active state before the expiration of a timer of which the value is in the range of 500 ms to 1 s.

NOTE 6: Applicable only for TEs which are locally powered and able to detect PS1 or PS2.

NOTE 7: If INFO 2 of INFO 4 is not recognised within 5 ms after the appearance of a signal, TE shall go to F5. The result is to be tested 5 ms after generation of the stimulus.

NOTE 8: For TEs which are locally powered and able to detect PS1 or PS2, at the event "disappearance of power" in states F6 or F7, no state change shall be observed.

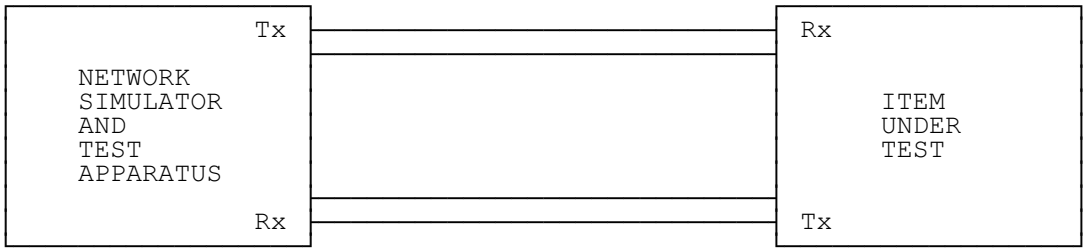
D.3.2.2 Timer for activation/deactivation (subclause A.6.2, ETS 300 012)

D.3.2.2.1 Timer for activation when receiving INFO 2

D.3.2.2.1.1 Test A, in state F3 (subclause A.6.2.6.1, ETS 300 012)

Purpose: To check the value of the TE activation times in the deactivated state.

Test configuration :



System state: Deactivated *(state F3)*.

Stimulus: INFO 2 type frames from the network.

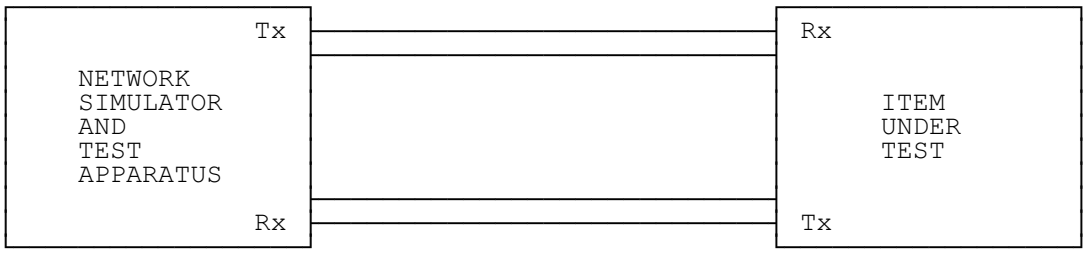
Monitor: The line signals with a digital storage oscilloscope, measuring the elapsed time between reception of INFO 2 and the subsequent transmission of INFO 3.

Results: INFO 3 is transmitted within 100 ms.

D.3.2.2.1.2 Test B, in state F4 (subclause A.6.2.6.1, ETS 300 012)

Purpose: To check the value of the TE activation times in the waiting for signal state.

Test configuration:



System state: Awaiting signal *(state F4)*.

Stimulus: INFO 2 type frames from the network.

Monitor: The line signals with a digital storage oscilloscope, measuring the elapsed time between:

a) reception of INFO 2 and cessation of INFO 1;

b) reception of INFO 2 and the subsequent transmission of INFO 3.

during activation by the terminal.

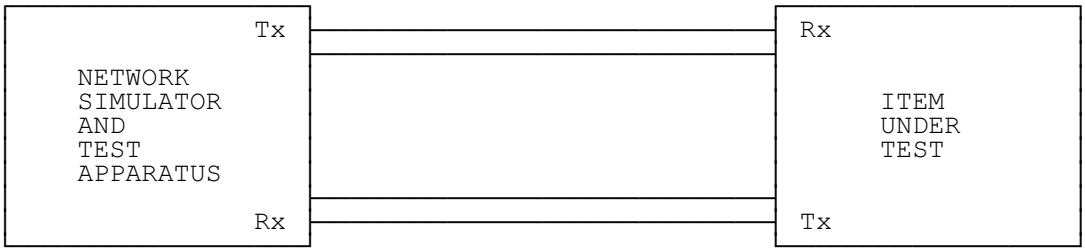
Results: INFO 1 ceases within 5 ms of the receipt of INFO 2 and INFO 3 is transmitted within 100 ms.

D.3.2.2.2 Timer for activation when receiving INFO 4 (subclause A.6.2, ETS 300 012)

D.3.2.2.2.1 Test A, in state F3 (subclause A.6.2.6.1, ETS 300 012)

Purpose: To check the value of the TE activation times in the deactivated state.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: INFO 4 type frames from the network.

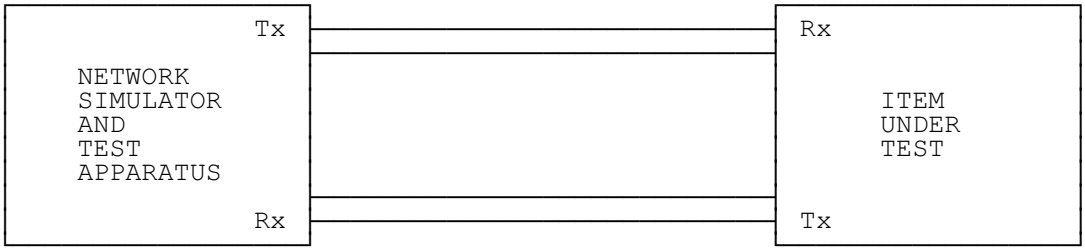
Monitor: The line signals with a digital storage oscilloscope, measuring the elapsed time between reception of INFO 4 and the subsequent transmission of INFO 3.

Results: INFO 3 is transmitted within 100 ms.

D.3.2.2.2.2 Test B, in state F4 (subclause A.6.2.6.1, ETS 300 012)

Purpose: To check the value of the TE activation times in the waiting for signal state.

Test configuration:



System state: Awaiting signal *(state F4)*.

Stimulus: INFO 4 type frames from the network.

Monitor: The line signals with a digital storage oscilloscope, measuring the elapsed time between:

a) reception of INFO 4 and cessation of INFO 1;

b) reception of INFO 4 and the subsequent transmission of INFO 3.

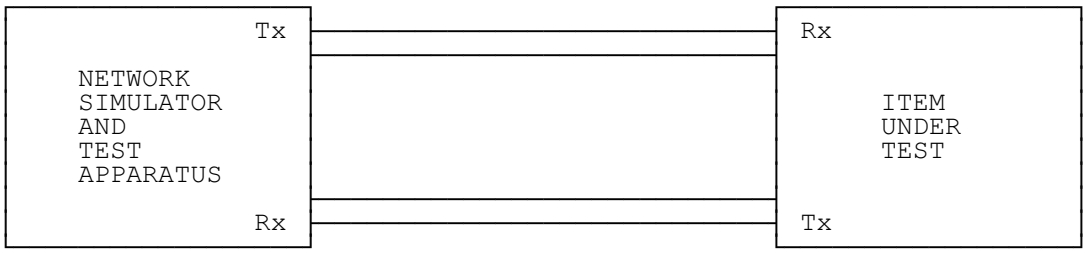
during activation by the terminal.

Results: INFO 1 ceases within 5 ms of the receipt of INFO 4 and INFO 3 is transmitted within 100 ms.

D.3.2.2.3 Timer for activation when receiving any signal (subclause A.6.2.6.1, ETS 300 012)

Purpose: To check the value of the TE activation times in the waiting for signal state.

Test configuration:



System state: Awaiting signal *(state F4)*.

Stimulus: Any signal type frames from the network.

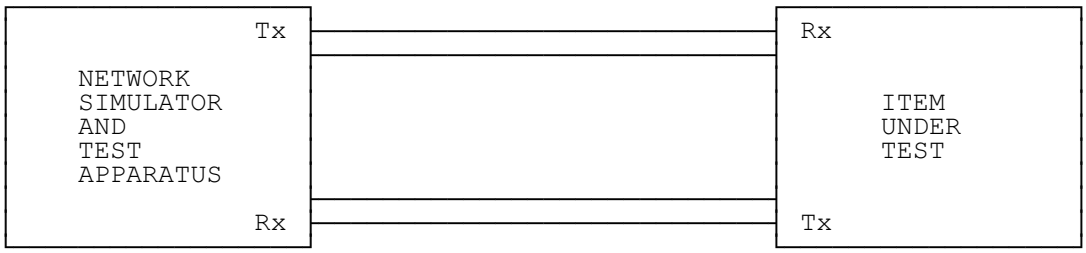
Monitor: The line signals measuring the elapsed time between reception of any signal and cessation of INFO 1.

Results: INFO 1 ceases within 5 ms of the receipt of any signal.

D.3.2.2.4 Value of the timer T3 (subclause A.6.2.5, ETS 300 012)

Purpose: To check the value of timer T3.

Test configuration :



System state: Awaiting signal *(state F4)*.

Stimulus: Activated by the IUT (PH-AR) activation request (this occurs during the normal activation procedure).

INFO 0 from the network (see NOTE 4 in subclause D.3.2.1).

Monitor: The line signals with a digital storage oscilloscope measuring the elapsed time between the beginning of INFO 1 and its cessation.

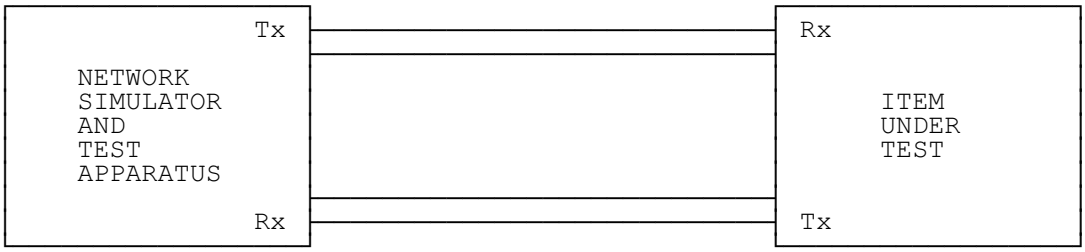
Results: Timer T3 shall not exceed 30 sec.

D.3.2.2.5 Timer for physical deactivation

D.3.2.2.5.1 Test A, in state F6 (subclause A.6.2.7, ETS 300 012)

Purpose: To check the value of the TE deactivation times.

Test configuration:



System state: Synchronised *(state F6)*.

Stimulus: INFO 0 from the network (see NOTE 4 in subclause D.3.2.1).

Monitor: The line signals measuring the elapsed time between :

- reception of INFO 0 and cessation of INFO 3 *(sending INFO 0)*.

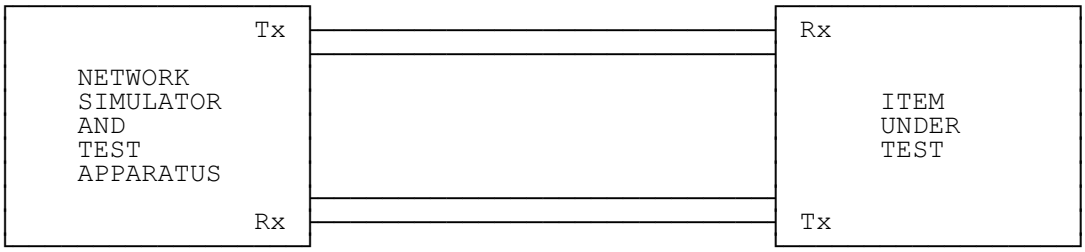
Results: INFO 3 ceases within 250 µs to 25 ms.

NOTE: the zero time reference point starts immediately after the 48th bit of the last received frame different from INFO 0.

D.3.2.2.5.2 Test B, in state F7 (subclause A.6.2.7, ETS 300 012)

Purpose: To check the value of the TE deactivation times.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: INFO 0 from the network (see NOTE 4 in subclause D.3.2.1).

Monitor: The line signals measuring the elapsed time between :

- reception of INFO 0 and cessation of INFO 3 *(sending INFO 0)*.

Results: INFO 3 ceases within 250 µs to 25 ms.

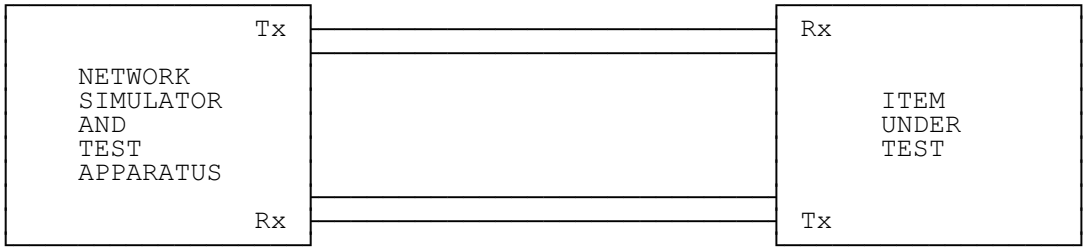
NOTE: The zero time reference point starts immediately after the 48th bit of the last received frame different from INFO 0.

D.3.2.2.6 Timer for complete deactivation

D.3.2.2.6.1 Test A, in state F7 (subclause A.6.2.3.2, ETS 300 012, NOTE 6)

Purpose: To check the value of the timer when leaving state F7 upon the reception of INFO 0.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: INFO 0 from the network simulator (see NOTE 4 in subclause D.3.2.1) and then to INFO 4.

Monitor: The ongoing communication.

Results: The value of the timer is in the range of 500 ms to 1000 ms.

If the duration of INFO 0 from the network is less than 500 ms : no loss of the ongoing communication.

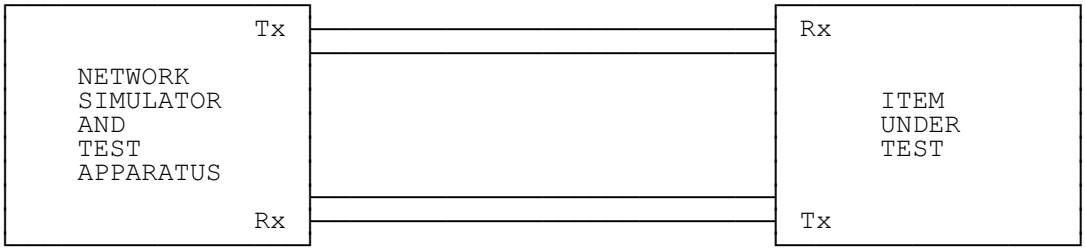
If the duration of INFO 0 from the network is greater than 1000 ms : loss of the ongoing communication.

NOTE: This test applies for IUT where layer 3 timer T.309 (defined in ETS 300 102-1 [13]) is not implemented.

D.3.2.2.6.2 Test B, in state F8 (subclause A.6.2.3.2, ETS 300 012, NOTE 6)

Purpose: To check the value of the timer when leaving state F8 upon the reception of INFO 0.

Test configuration:



System state: Lost framing *(state F8)*. With an ongoing communication established.

Stimulus: INFO 0 from the network simulator, (see NOTE 4 in subclause D.3.2.1).

Monitor: The ongoing communication.

Results: The value of the timer is in the range of 500 ms to 1000 ms.

If the duration of INFO 0 from the network is less than 500 ms : no loss of the ongoing communication.

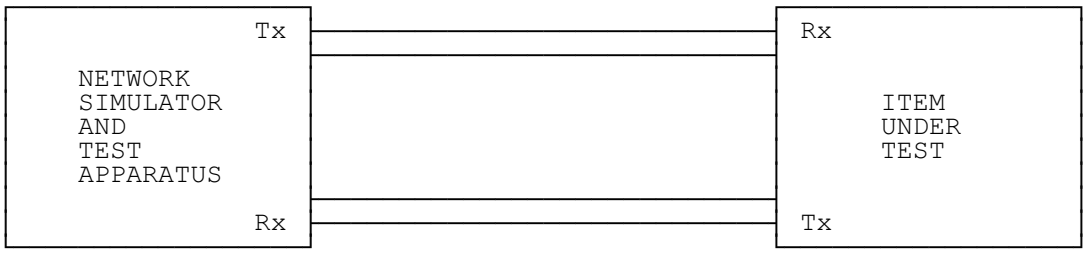
If the duration of INFO 0 from the network is greater than 1000 ms : loss of the ongoing communication.

NOTE: This test applies for IUT where layer 3 time T309 (defined in ETS 300 102-1 [13]) is not implemented.

D.3.3 Frame alignment procedures (subclause A.6.3, ETS 300 012)

Purpose: To test the IUT correctly executes the frame alignment procedures.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: Good/bad frames from the network simulator.

NOTE 1: A bad frame is simulated by any bit pattern on which the IUT conforming to subclause A.6.3.1.2 of ETS 300 012 is not able to synchronise.

NOTE 2: The start of a frame is defined to the position where the F-bit according to figure 3/I.430 [2] should appear.

Monitor: Line signals INFO 3 received from the IUT at the network simulator.

Results :

	STIMULUS	**RESULTS**	**COMMENTS**
a)	1 bad frame	INFO 3	No loss of framing
b)	n bad frames *(NOTE 3)*	INFO 0	Framing lost
c)	m good frames *(NOTE 4)*	INFO 3	Framing regained within m+1 frames

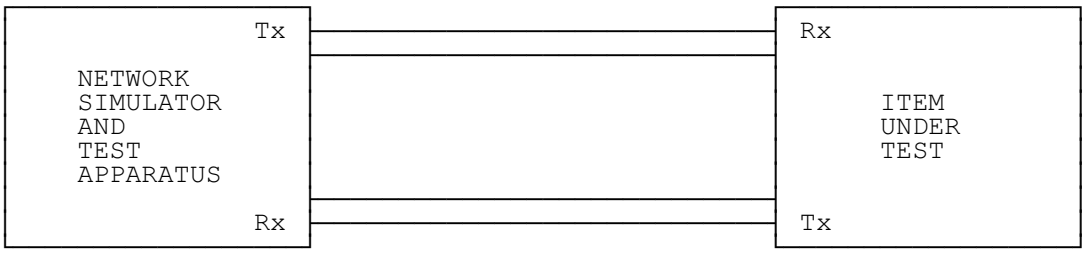
NOTE 3: The value of n ($n \geq 2$) shall be provided by the supplier of the IUT before the test.

NOTE 4: Before the test, the TE shall be in state F8. The input shall be applied with "Any signal". Multiframing is not covered by this test. The value of m (corresponding to at least 3 consecutive pairs of line code violations) shall be provided the supplier of the IUT before the text.

D.3.4 Multiframing procedures (subclause A.6.3.3, ETS 300 012)

Purpose: To test the IUT correctly executes the multiframing procedures.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: Transmission of the Fa/N bit pairs from the network simulator indicating normal and the multiframe bit sequence.

Normal	Fa = ZERO	N = ONE
Multiframe	Fa = ONE	N = ZERO

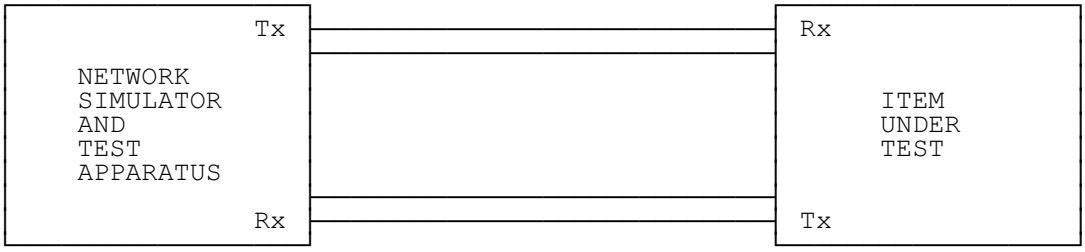
Monitor: Line signals INFO 3 received from the IUT at the network simulator.

Results: When network sends Fa = ZERO, returned Fa from IUT = ZERO,
When network sends Fa = ONE, returned Fa from IUT (Q bit) = ONE.

D.3.5 Idle channel code on the B-channels (subclause A.6.4, ETS 300 012)

Purpose: To check the contents of all non-assigned B-channels.

Test configuration:



System state: Activated *(State F7)*.

Stimulus: INFO 4.

Monitor: B-channel at the monitor port of the network simulator.

Results: Binary ONEs.

D.4 Electrical characteristics tests (Clause A.8, ETS 300 012)

These tests check that the interface conforms to the electrical characteristics specified in Clause A.8 of ETS 300 012.

Many of these tests require the interface to be stable in the activated state and transmitting a specific bit pattern, both with or without the connection to the NT1 receiving pair. As none of these requirements can be met with the network simulator operating normally it is anticipated that special arrangements will be made to permit this, for example the receiving section to the NT1 could be manually set in the appropriate state.

There is also the restriction imposed by access to the TEs B-channels.

The characteristics measured by these tests may vary with the type of power source or power sink and the extremes of voltage provided by the network. It is therefore necessary to repeat the tests at the extremes of DC voltage levels, minimum and maximum, for local power, normal power and restricted power conditions.

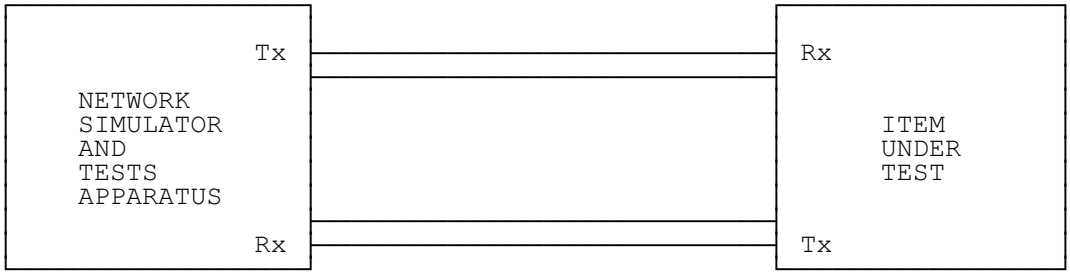
Moreover the IUT shall meet the specified electrical characteristics in conformance with the requirements of subclause D.1.1 of this document.

When a Power Source 1 is used, its effect shall be taken into account in the test methodology.

D.4.1 Frame rate when transmitting an INFO 1 (subclause A.8.1, ETS 300 012)

Purpose: The average frame rate when the TE is transmitting INFO 1 type frames.

Test configuration:



System state: Awaiting signal *(state F4)*.

Stimulus: INFO 0 type frames from the network (see NOTE 4 in subclause D.3.2.1).

Monitor: Frame rate.

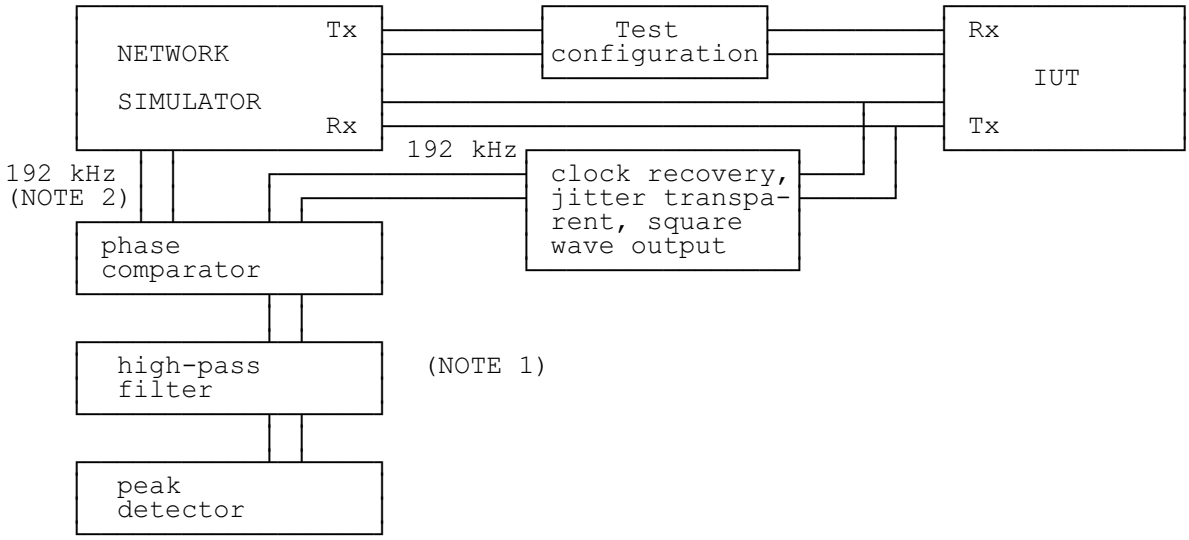
Results: Nominal frame rate of 24 kHz ± 100 ppm.

D.4.2 TE jitter characteristics (subclause A.8.2, ETS 300 012)

TE jitter measurement characteristics *(test A)* (subclause A.8.2.2, ETS 300 012)

Purpose: TE output jitter when transmitting INFO 3 type frames.

Test configuration: See the subclause A.8.2.1, ETS 300 012 for test configurations.



System state: Activated *(state F7)*.

Stimulus: INFO 4 type frames from the network containing :

a) All binary ONEs in D, D-echo and both B-channels.

b) A sequence repeated continuously for at least 10 seconds consisting of:

- 40 frames with continuous octets of 10101010 *(the first bit to be transmitted is a binary ONE)*, in both B-channels and continuous binary ONEs in the D and D-echo channels followed by:

- 40 frames with continuous binary ZEROs in D, D-echo and both B channels.

c) A sequence consisting of pseudo random pattern with a length of 2^{19}-1 in D, D-echo and both B-channels.

Monitor: Peak-to-peak jitter measured using a peak detector through a high-pass filter and a phase comparator. The filter shall have a low-cut frequency *(3 dB point)* of 30 Hz and an asymptotic roll-off of 20 dB per decade. One input of the phase comparator shall be a 192 kHz signal synchronous with the NT simulator, the other input shall be a square wave signal at 192 kHz extracted from the analogue signal transmitted from the IUT. To obtain this digital signal a square wave generator can be used triggered by all the zero crossing transitions of all adjacent binary ZEROs.

The block diagram in the figure is only a logical representation and it does not represent an actual implementation.

NOTE 1: For measurement purposes an additional low-pass filter with a cut-off frequency higher than 96 kHz can be added. (See CCITT Recommendation O.171 [14]).

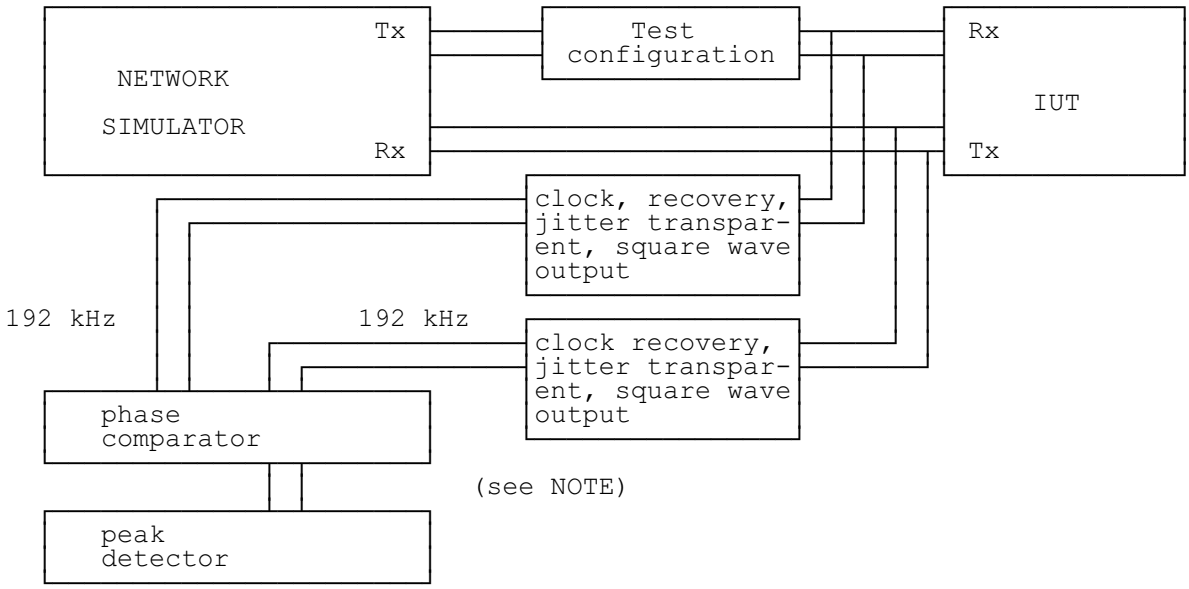
NOTE 2: the clock provided by the network simulator shall be synchronous with the signal received by the Item Under Test.

Results: The maximum jitter shall be less than ± 7 % of a bit period.

D.4.2.2 TE output phase deviation *(test B)* (subclause A.8.2.3, ETS 300 012)

Purpose: TE total phase deviation input to output.

Test configuration: See subclause A.8.2.1, ETS 300 012 for test configurations.



System state: Activated *(state F7)*.

Stimulus: INFO 4 type frames from the network containing:

a) A sequence consisting of continuous frames with all binary ONEs in the D, D-echo and both B-channels.

b) A sequence consisting of continuous frames with the octet "10101010" *(the first bit to be transmitted is binary ONE)* in both B-channels and binary ONEs in D and D-echo channel.

c) A sequence of continuous frames with binary ZEROs in D, D-echo and both B-channels.

d) A sequence of continuous frames with a pseudo-random pattern, as described in ETS 300 012/subclause A.8.2.2 c), in D, D-echo and both B-channels.

Superimposed jitter as specified in figure 10/I.430 [2] over the range of frequencies from 5 Hz to 2 kHz shall also be applied to the input signal from the network.

Monitor: Peak to peak jitter measured using a peak voltmeter through an additional low-pass filter *(see note)* and a phase comparator (see CCITT Recommendation Q.171 [14]).

One input of the phase comparator shall be a 192 kHz signal synchronous with the NT simulator, the other input shall be a square wave signal extracted at 192 kHz from the analogue signal transmitted from the IUT. To obtain this digital signal a square wave generator can be used triggered by all the zero crossing transitions of all adjacent binary ZEROs.

The block diagram in the figure is only a logical representation and it does not represent an actual implementation.

NOTE: For measurement purposes an additional low-pass filter with a cut-off frequency higher than 96 kHz can be added (see CCITT Recommendation O.171 [14]).

Results: The maximum phase deviation shall be - 7 % ≤ X ≤ 15 % of a bit period.

(This phase deviation does not include the two-bit period between transmitted and received frames).

The measured deviation Y with included two bit period is equivalent to: 10,05 µs ≤ Y ≤ 11,20 µs

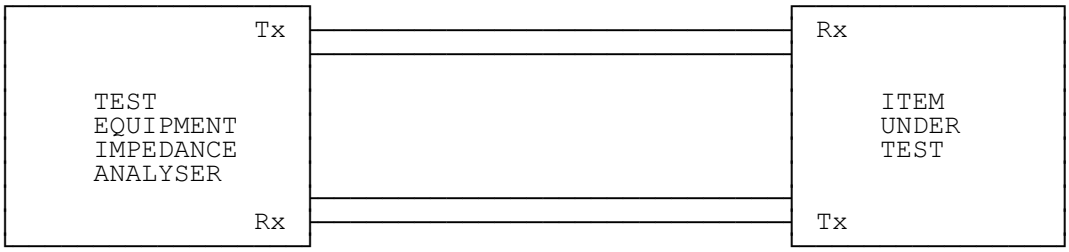
D.4.3 TE transmitter output impedance (subclause A.8.5.1.2, ETS 300 012)

D.4.3.1 Test A

Purpose: Output impedance of the transmitters when transmitting a binary ONE *(no signal)*.

NOTE : This requirement also applies to the APS.

Test configuration:



System state: Deactivated*(state F3)*.

Stimulus: Sinusoidal voltages of 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

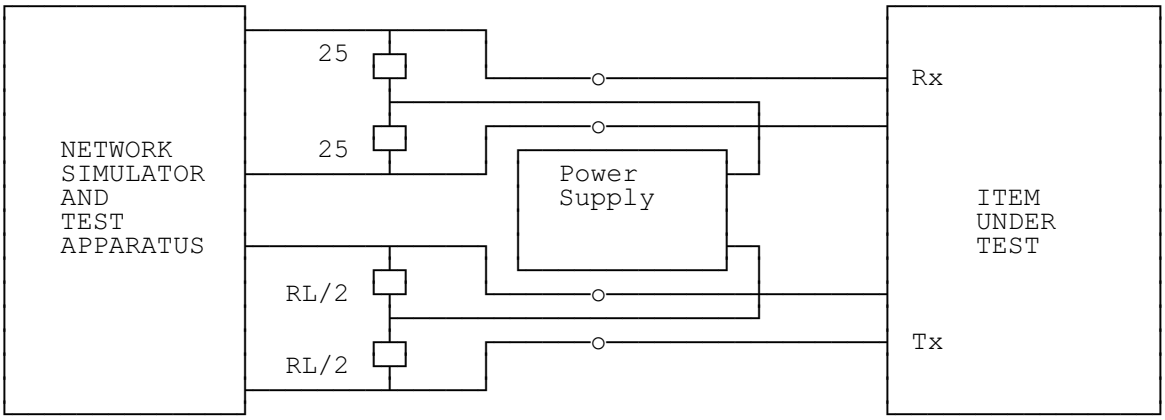
Monitor: Impedance.

Results: The measured value shall exceed the impedance template of figure 12/I.430 [2].

D.4.3.2 Test B

Purpose: Output impedance of the transmitters when transmitting a binary ZERO.

Test configuration:



System state: Activated *(state F7)*.IUT transmitting positive and negative pulses into a load resistance *(see subclause D.1 of this document)*.

Stimulus: INFO 4.

Monitor: Both positive and negative pulses.

The output impedance limit shall apply for 2 nominal load impedance *(resistive)* conditions : RL = 50 and 400 ohms. The output impedance for each nominal load is defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10 %. The peak amplitude is defined as the amplitude of the midpoint of the pulse. The test applies for pulses of both polarities.

Results: The output impedance shall be ≥ 20 ohms

$$R = \frac{U_+ - U_-}{U_-/R_- - U_+/R_+}$$

R_+ : nominal resistance R_L + 10 %.
R_- : nominal resistance R_L - 10 %.

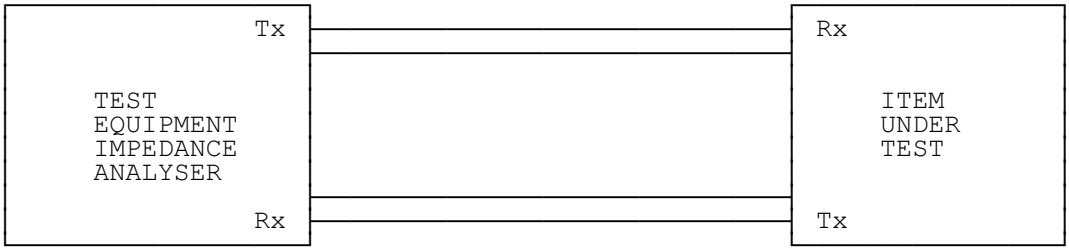
U_+ : peak amplitude when R_+ is applied.
U_- : peak amplitude when R_- is applied.

D.4.3.3 Test C

Purpose: Output peak current.

NOTE: This requirement also applies to the APS.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Sinusoidal voltage up to 1,2 V (peak value) at a frequency of 96 kHz (the applied voltage to be monitored with oscilloscope to ensure peak values are correct).

Monitor: Peak current.

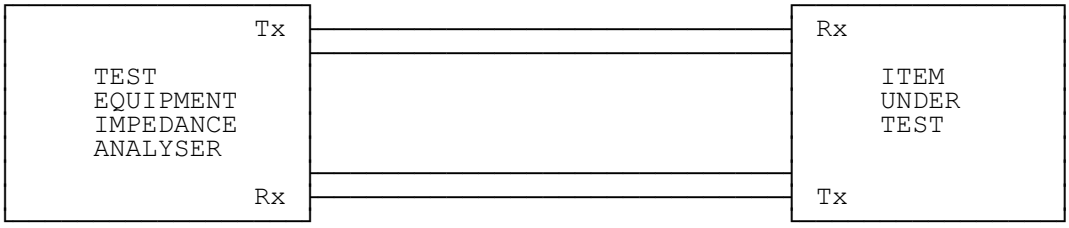
Results: Peak current shall not exceed 0,6 mA.

D.4.3.4 Test D

Purpose: Output impedance of the transmitters in the inactive state.

NOTE : This requirement also applies to the APS.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Sinusoidal voltage of 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

Monitor: Impedance.

Results: The measured value shall exceed the impedance template of figure 12/I.430 [2].

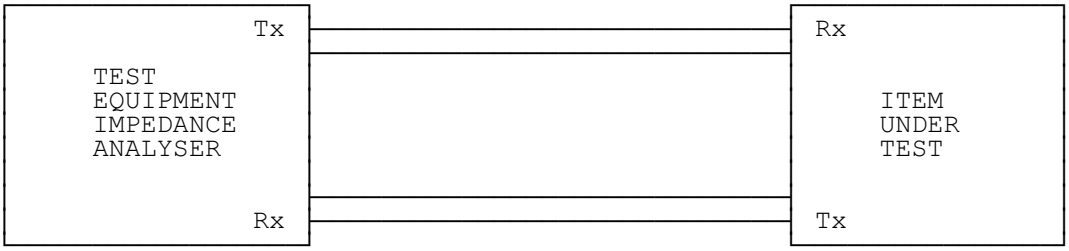
When the IUT is a locally powered TE able to detect power source 1 or 2, two tests shall be performed *(powered off/power on without PS1 and PS2)*.

D.4.3.5 Test E

Purpose: Output peak current.

NOTE: This requirement also applies to the APS.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Sinusoidal voltage of 1,2 V (peak value) at a frequency of 96 kHz (the applied voltage to be monitored to ensure peak values are correct).

Monitor: Peak current.

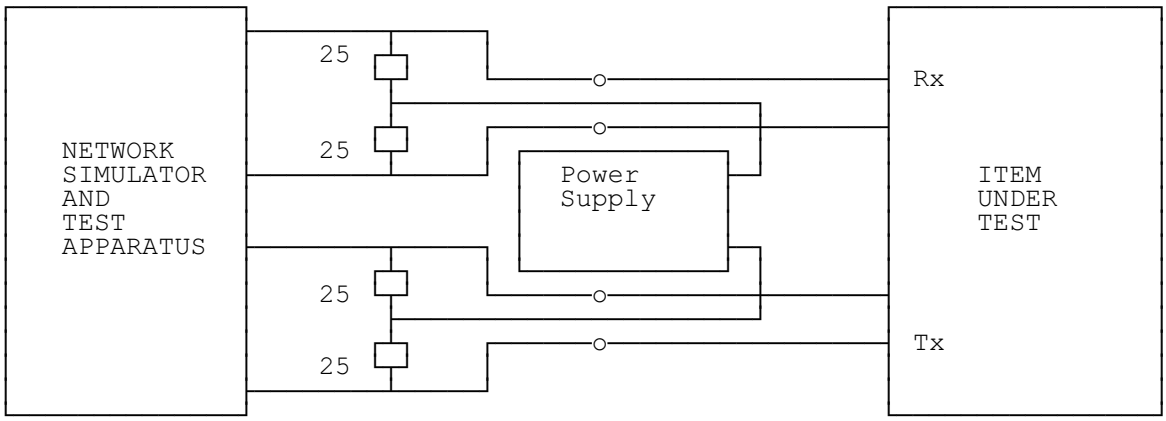
Results: Peak current shall not exceed 0,6 mA.

When the IUT is a locally powered TE able to detect power source 1 or 2, two tests shall be performed *(powered off/power on without PS1 and PS2)*.

D.4.4 Pulse shape and amplitude (subclause A.8.5.3, ETS 300 012)

Purpose: Pulse shape and amplitude of isolated transmitted pulses.

Test configuration:



User/network interface transmitting pair terminated in 50 ohm terminating resistor, i.e. NT1 receiving circuiting connected without its terminating resistor.

System state: Activated *(state F7)*.

IUT transmitting isolated pulses *(no adjacent pulses)* into a normally terminated bus *(see Clause D.1)*.

Stimulus: Isolated pulses of normal amplitude.

Monitor: Both positive and negative pulses.

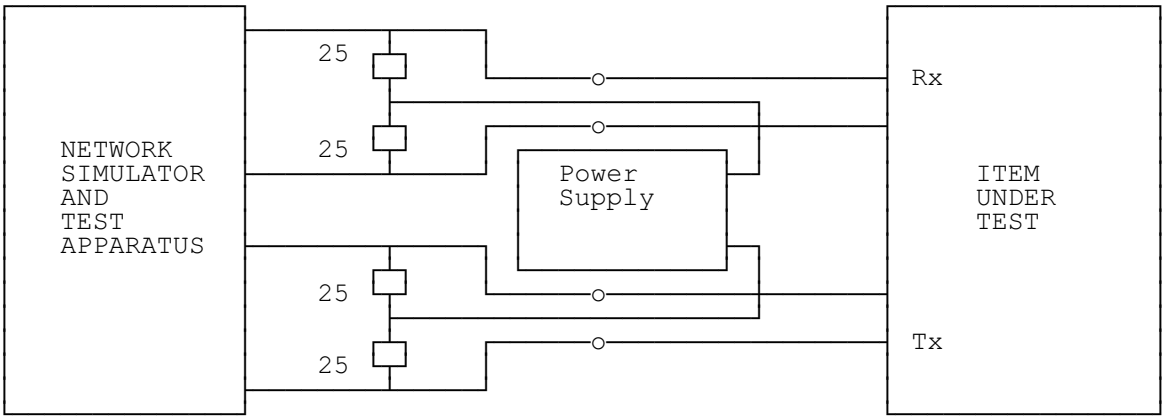
Results: Both positive and negative pulses shall be within the mask of figure 13/I.430 [2] with a nominal amplitude of 750 mV zero to peak *(also see subclause A.8.5.3.1, ETS 300 012)*.

D.4.5 Pulse unbalance (subclause A.8.5.4, ETS 300 012)

D.4.5.1 Pulse amplitude (subclause A.8.5.4.1, ETS 300 012)

Purpose: Pulse amplitude when transmitting a high density pattern.

Test configuration:



System state: Activated *(state F7)*.

IUT transmitting INFO 3 with both B-channels filled with binary ZEROs.

Stimulus: INFO 4.

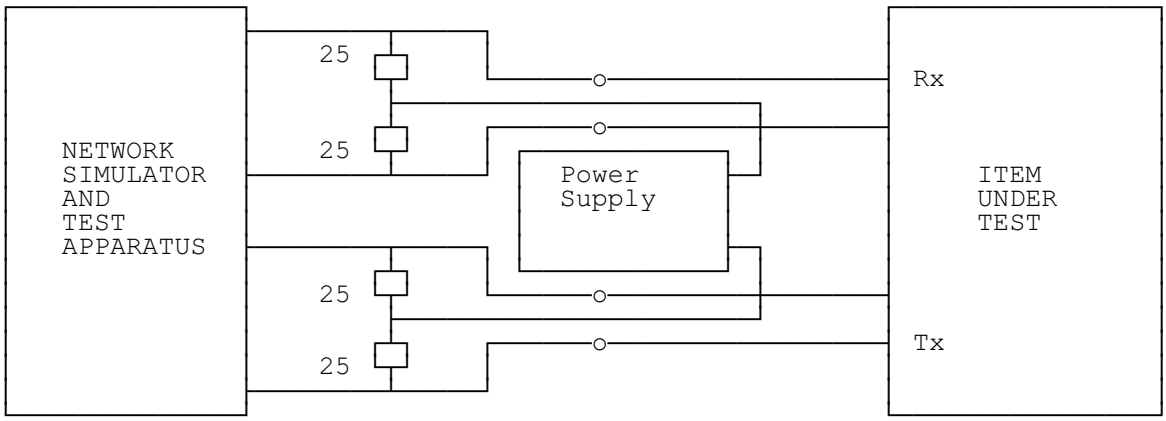
Monitor: The amplitude of positive and negative pulses at the midpoint of the pulse.

Results: All pulses amplitude of 40 continuous frames in the midpoint of the pulse shall be within the ± 10 % of the nominal amplitude values.

D.4.5.2 Pulse unbalance of an isolated couple of pulses (subclause A.8.5.4.2, ETS 300 012)

Purpose: The relative difference in integral Udt for a positive and negative pulse.

Test configuration:



System state: a) Deactivated *(state F3)*, then

b) Synchronised *(state F6)*.

IUT transmitting INFO 3 containing all binary ONEs in both B-channels and in the D-channel *(see Clause D.1)*.

Stimulus: INFO 2.

Monitor: a) voltage when transmitting INFO 0.

b) First isolated couple of pulses following INFO 0.

Results: The relative difference (*NOTE*) in integral Udt for a positive pulse and the integral Udt for a negative pulse shall be less than 5 % of the nominal pulse. The zero reference voltage is given by the signal when transmitting INFO 0.

NOTE: The edge between the two adjacent pulses is the crossing of the zero voltage. From this edge, the integral is defined for a time period of 1,5 UI in each direction.

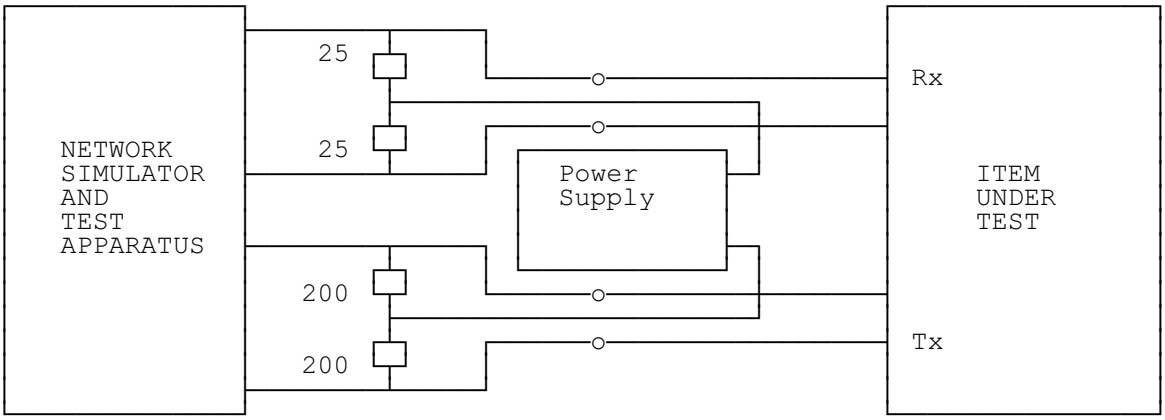
D.4.6 Voltage on other test loads (subclause A.8.5.5, ETS 300 012)

Purpose: To ensure compatibility where multiple TEs are transmitting.

D.4.6.1 Test A (subclause A.8.5.5.1, ETS 300 012)

Purpose: Voltage, on a 400 ohm test load, to prevent pulses adding when 2 to 8 drivers are in parallel.

Test configuration:



System state: Activated *(state F7)*.

TE transmitting isolated pulses *(no adjacent pulses)* into a 400 ohm load. (See Clause D.1).

Stimulus: INFO 4.

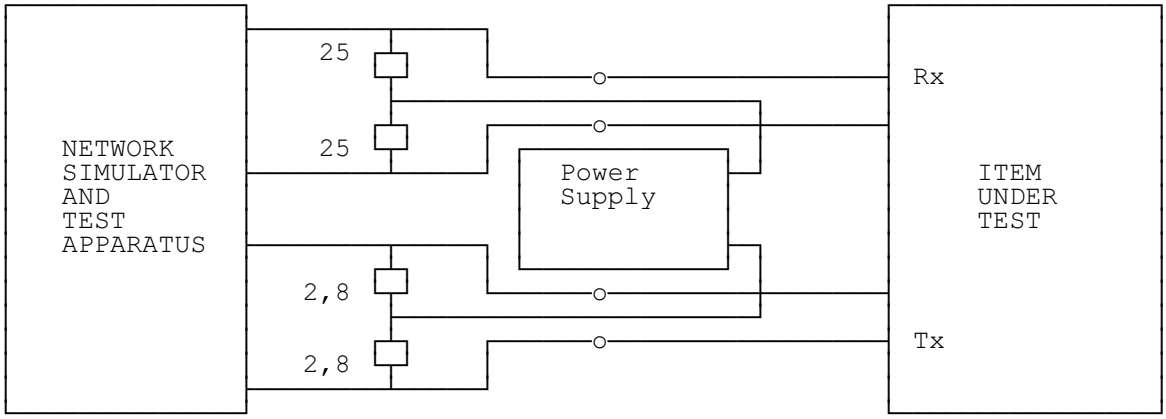
Monitor: Both positive and negative pulses.

Results: The pulses shall fit into the mask defined in figure 14/I.430 [2].

D.4.6.2 Test B (subclause A.8.5.5.2, ETS 300 012)

Purpose: Voltage on a 5,6 ohm test load, to prevent current flow when two opposite polarity drivers are in parallel.

Test configuration:



System state: Activated *(state F7)*.

Transmitting isolated pulses *(no adjacent pulses)* into 5,6 ohm load *(see Clause D.1)*

Stimulus: INFO 4.

Monitor: Both positive and negative pulses.

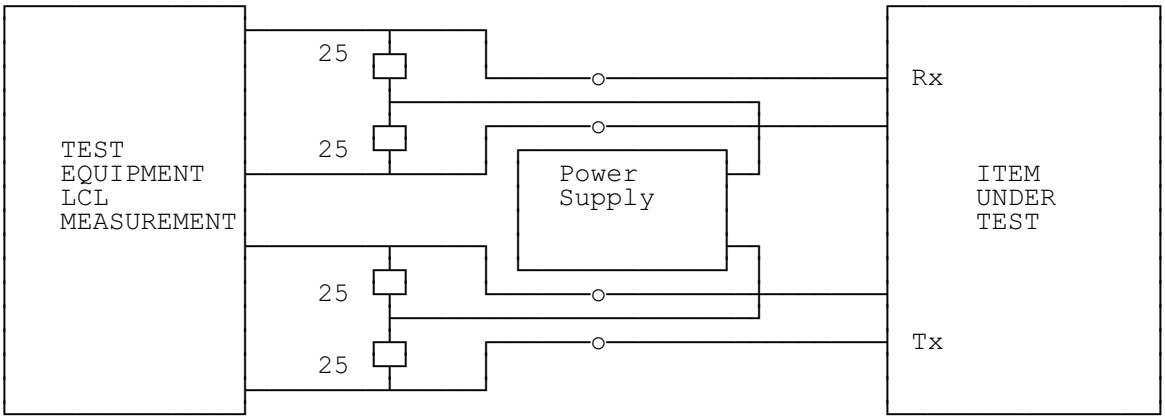
Results: The measured pulses shall be ≤ 20 % of the nominal pulse amplitude.

D.4.7 Longitudinal conversion loss of transmitter output (subclause A.8.5.6.1, ETS 300 012)

NOTE: These requirements also apply to the APS.

Purpose: Longitudinal Conversion Loss (LCL) (the ratio of longitudinal signal converted to a transverse signal as a result of the unbalance about earth of the terminal output).

Test configuration:



Measurement test configuration: See figure 15, I.430 [2].

System state: a) Deactivated *(state F3)*.

b) Inactive *(state F1)*.

Stimulus: One volt rms longitudinal in accordance with figure 15/I.430 [2].

Monitor: Transverse voltage in accordance with figure 15/I.430 [2] with selective level measuring instrument.

Results: 10 kHz ≤ f ≤ 300 kHz : ≥ 54 dB
300 kHz < f ≤ 1 MHz : minimum value decreasing from 54 dB at 20 dB/decade.

D.4.8 Receiver input characteristics (subclause A.8.6, ETS 300 012)

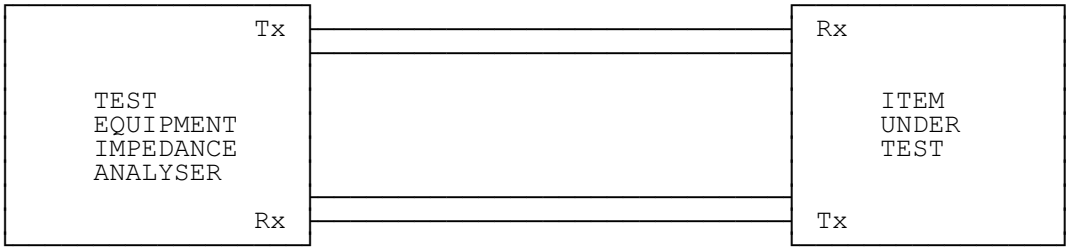
D.4.8.1 TE receiver input impedance (subclause A.8.6.1.1, ETS 300 012)

NOTE: These requirements also apply to the APS.

D.4.8.1.1 Test A

Purpose: To test the input impedance of terminals whilst in a deactive state.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Sinusoidal voltage of at least 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

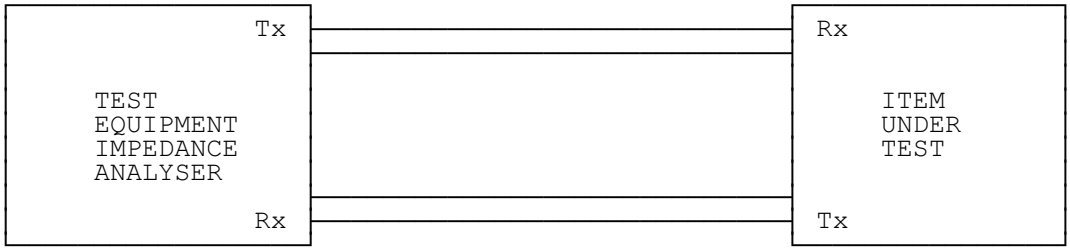
Monitor: Impedance.

Results: Shall exceed the impedance template of figure 12/I.430 [2].

D.4.8.1.2 Test B

Purpose: To test that the input impedance of the receiver when receiving an overvoltage signal is correct.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Sinusoidal voltage up to 1.2 V (peak value) at a frequency of 96 kHz (the applied voltage to be monitored to ensure peak values are correct).

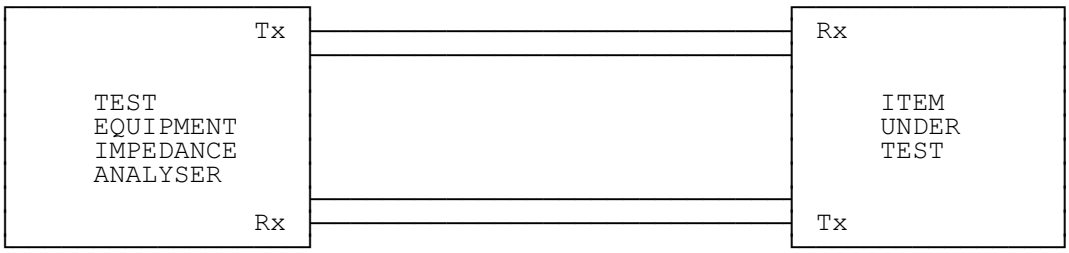
Monitor: Peak value of current.

Results: The peak current shall not exceed 0,6 mA peak value.

D.4.8.1.3 Test C

Purpose: To test the input impedance of TE receivers in the inactive state.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Sinusoidal voltage of at least 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

Monitor: Impedance.

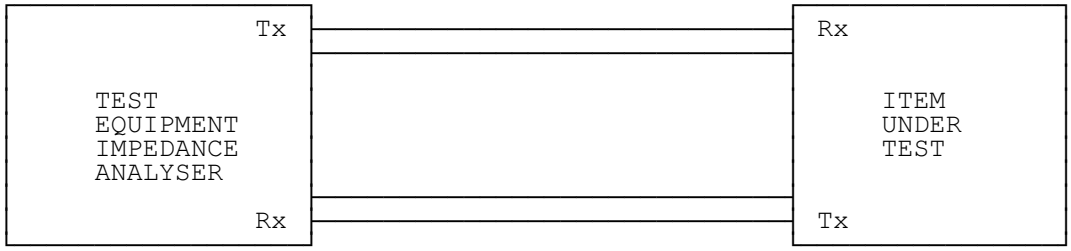
Results: Shall exceed the impedance template of figure 12/I.430 [2].

When the IUT is a locally powered TE able to detect power source 1 or 2, two tests shall be performed *(powered off/powered on without PS1 and PS2)*.

D.4.8.1.4 Test D

Purpose: To test that the input impedance of the receiver when receiving an overvoltage signal is correct.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Sinusoidal voltage up to 1,2 V (peak value) at a frequency of 96 kHz (the applied voltage to be monitored to ensure peak values are correct).

Monitor: Peak value of current.

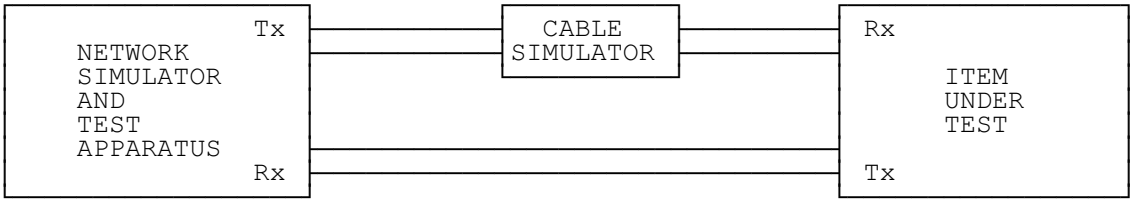
Results: The peak current shall not exceed 0,6 mA peak value.

When the IUT is a locally powered TE able to detect power source 1 or 2, 2 tests shall be done *(powered off/powered on without PS1 and PS2)*.

D.4.8.2 Receiver sensitivity - noise and distortion immunity (subclause A.8.6.2, ETS 300 012)

Purpose: Subclause A.8.6.2, ETS 300 012 is designed to correctly test the receivers function in the various wiring configurations.

Test configuration:



When performing this test the error rate measurement can be made either after the receiver using a B-channel access port or at the TE transmitter. If the measurement is at the TE transmitter, then the connection to the NT receiver should be in the ideal test configuration.

System state: Activated *(state F7)*.

Stimulus: Input signals are transmitted from the network simulator with a pseudo-random sequence *(word length ≥ 511 bits)* in both B-channels with amplitudes, delay and interfering signals as detailed in subclause A.8.6.2.1, ETS 300 012.

The following amplitudes are provided by the NT simulator corresponding to the bus configuration as given in subclause A.8.2.1, ETS 300 012.

Configuration	Amplitude relative to the nominal one
i (see NOTE)	- 1,5 dB at the NT simulator output
ii	- 1,5 dB and + 1,5 dB at the NT sim. output
iii	- 1,5 dB and + 1,5 dB at the NT sim. output
iv	+ 1,5 dB at the NT simulator output
NOTE: Additionally, the TEs shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak value) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals along with jitter.	

In addition, for each configuration jitter up to the maximum permitted *(subclause A.8.3, ETS 300 012)* in the output signal of NTs is superimposed on the input signals.

Monitor: B-channels from IUT checking the error rate *(see Clause D.1)*.

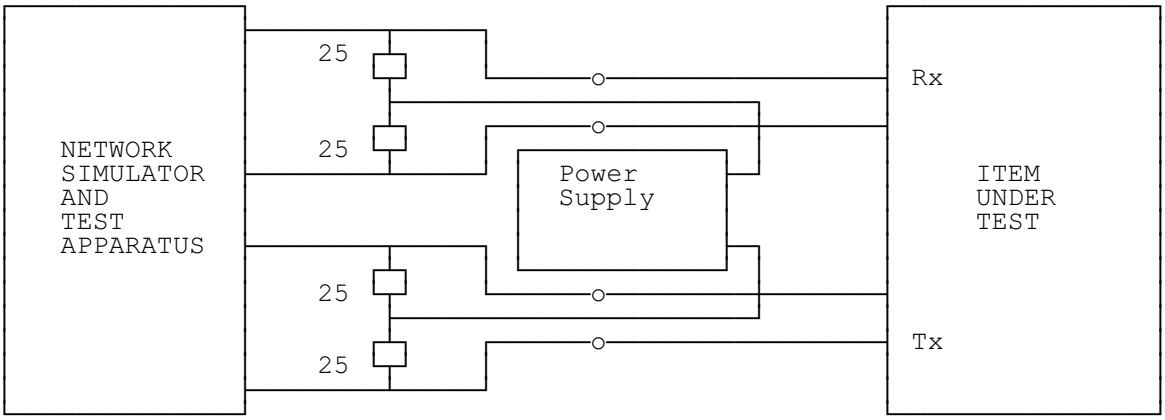
Results: No error for a monitoring period of at least one minute.

D.4.8.3 Unbalance about earth of receiver input (subclause A.8.6.4, ETS 300 012)

NOTE: These requirements also apply to the APS.

Purpose: Longitudinal Conversion Loss (LCL) (the ratio of longitudinal signal converted to a transverse signal as a result of the unbalance about earth of the terminal output).

Test configuration:



Measurement test configuration: See figure 15, CCITT Recommendation I.430 [2].

System state: a) Deactivated *(state F3)*.

b) Inactive *(state F1)*.

Stimulus: 1 volt rms longitudinal in accordance with figure 15/I.430 [2].

Monitor: Transverse voltage in accordance with figure 15/I.430 [2] with selective level measuring instrument.

Results: 10 kHz ≤ f ≤ 300 kHz : ≥ 54 dB
300 kHz < f ≤ 1 MHz : minimum value decreasing from 54 dB at 20 dB/decade.

D.5 Power feeding (subclause A.9, ETS 300 012)

The different values concerning consumption are given in table 8, I.430 [2].

Power feeding tests assume the following conditions:

a) An IUT may be in any state of activation.

b) An IUT may be making or receiving a call.

c) At no stage of an active call may the defined values be exceeded.

- The test conditions corresponding to the maximum consumption state are under study.

- All the values referring to power in Watts shall be measured using an instrument which integrates the measurements over a period of 50 ms.

- When measuring power consumption, the power loss due to resistance in the line and the feeding transformers shall be subtracted. However, power loss due to resistance in the line transformers in the TE and in the TE cord shall not be subtracted.

- For testing purposes, no power shall be interpreted as the TE consuming not more than 10 micro amps *(this gives allowance for leakage losses and inefficiencies)*.

- For the simulator, all rise times or fall times of voltage are defined between 90 % and 10 % of the voltage measured with resistive load without the IUT connected.

The requirements shall be met in all of the above conditions.

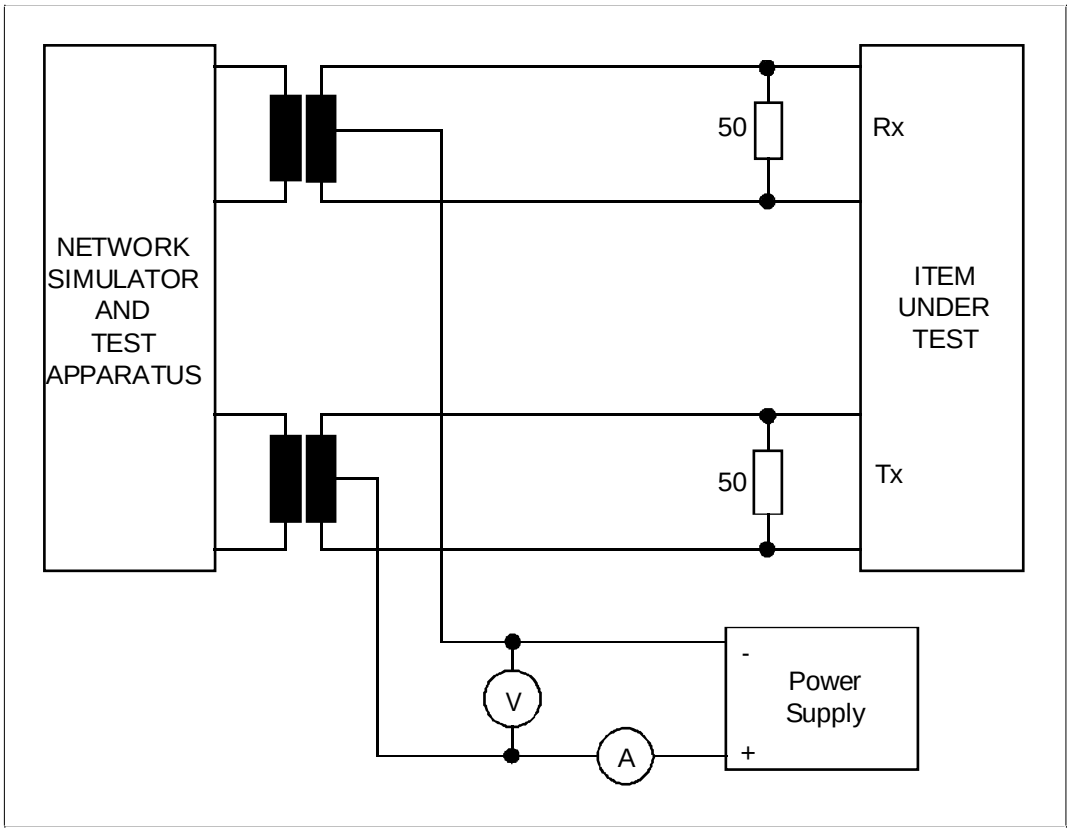
D.5.1 Power source 1 phantom mode (subclause A.9.3.1, ETS 300 012)

D.5.1.1 Normal power conditions (subclause A.9.3.1.1, ETS 300 012)

D.5.1.1.1 Normal power provision (Test A)

Purpose: To ensure an ACTIVATED TE does not draw excessive power from a normal mode, phantom Power Source 1, whilst in an activated state.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: Phantom, normal Power Source 1 in the voltage range 40 V, + 5 %/- 40 % *(42 V to 24 V)*.

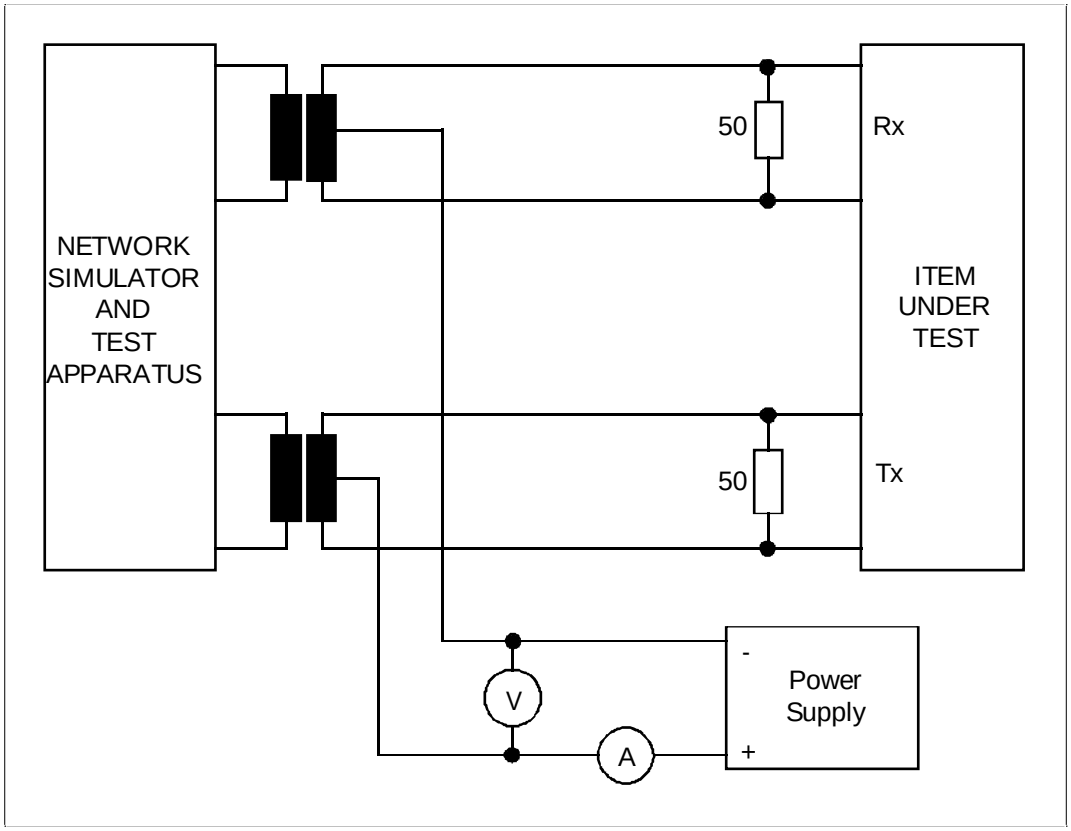
Monitor: DC voltage and current.

Results: The power drawn *(V * I)* shall not exceed 1 Watt at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.1.2 Normal power provision (Test B)

Purpose: To ensure the DEACTIVATED TE does not draw excessive power from a normal mode, phantom Power Source 1.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Phantom, normal mode Power Source 1 in the voltage range 40 V, +5 %/ - 40 % (*42 V to 24 V)*.

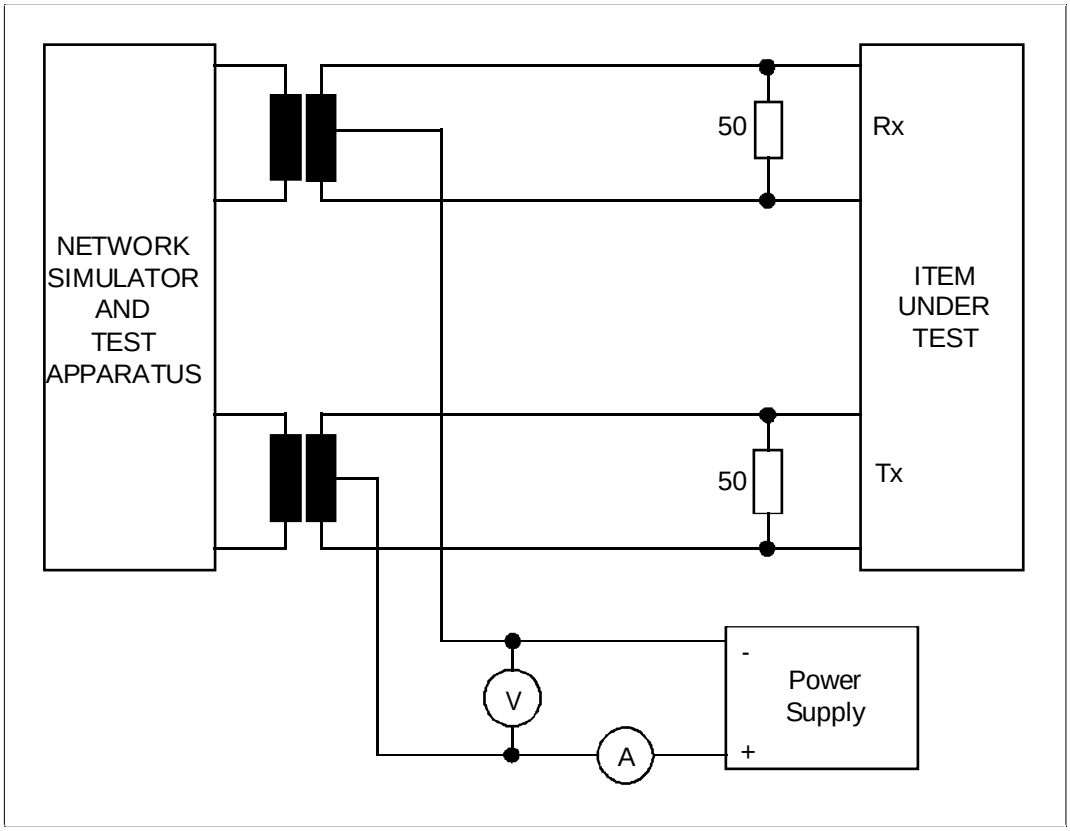
Monitor: DC voltage and current.

Results: The power drawn (*V * I*) shall not exceed 100 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.1.3 Normal power provision (Test C)

Purpose: To ensure a DEACTIVATED TE does not draw excessive power from a normal mode, phantom Power Source 1, whilst in local action.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Local action. Phantom, normal mode Power Source 1 in the voltage range 40 V, + 5 %/- 40 % *(42 V to 24 V)*.

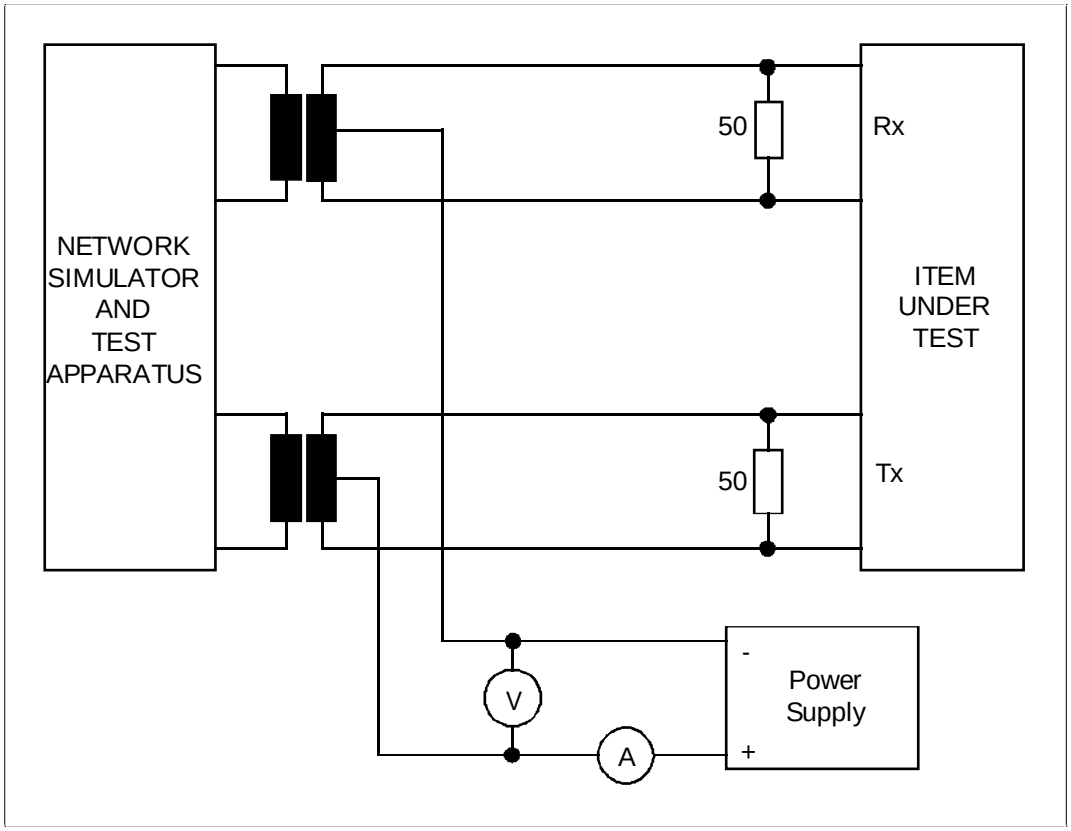
Monitor: DC voltage and current.

Results: The power drawn *(V * I)* shall not exceed 1 Watt at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.1.4 Normal power provision (Test D)

Purpose: To ensure a LOCALLY POWERED TE using connected detector does not consume excessive power in any state from PS1.

Test configuration:



System state: Any state.

Stimulus: Phantom, normal mode Power Source 1 in the voltage range 40 V, + 5 %/- 40 % (*42 V to 24 V*).

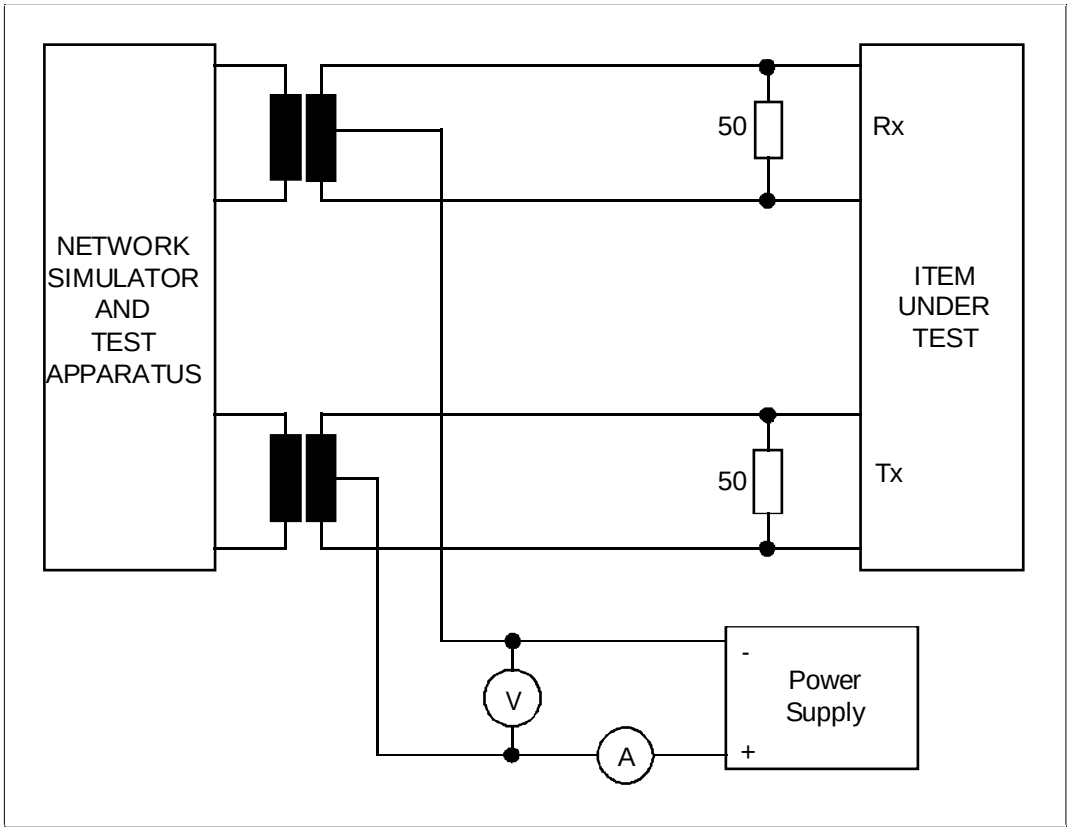
Monitor: DC voltage and current.

Results: The power consumed by the TE shall not exceed 3 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.1.5 Normal power provision (Test E)

Purpose: To ensure a LOCALLY POWERED TE not using connected detector does not consume power in any state from PS1.

Test configuration:



System state: Any state.

Stimulus: Phantom, normal mode Power Source 1 in the voltage range 40 V, + 5 %/- 40 % *(42 V to 24 V)*.

Monitor: DC voltage and current.

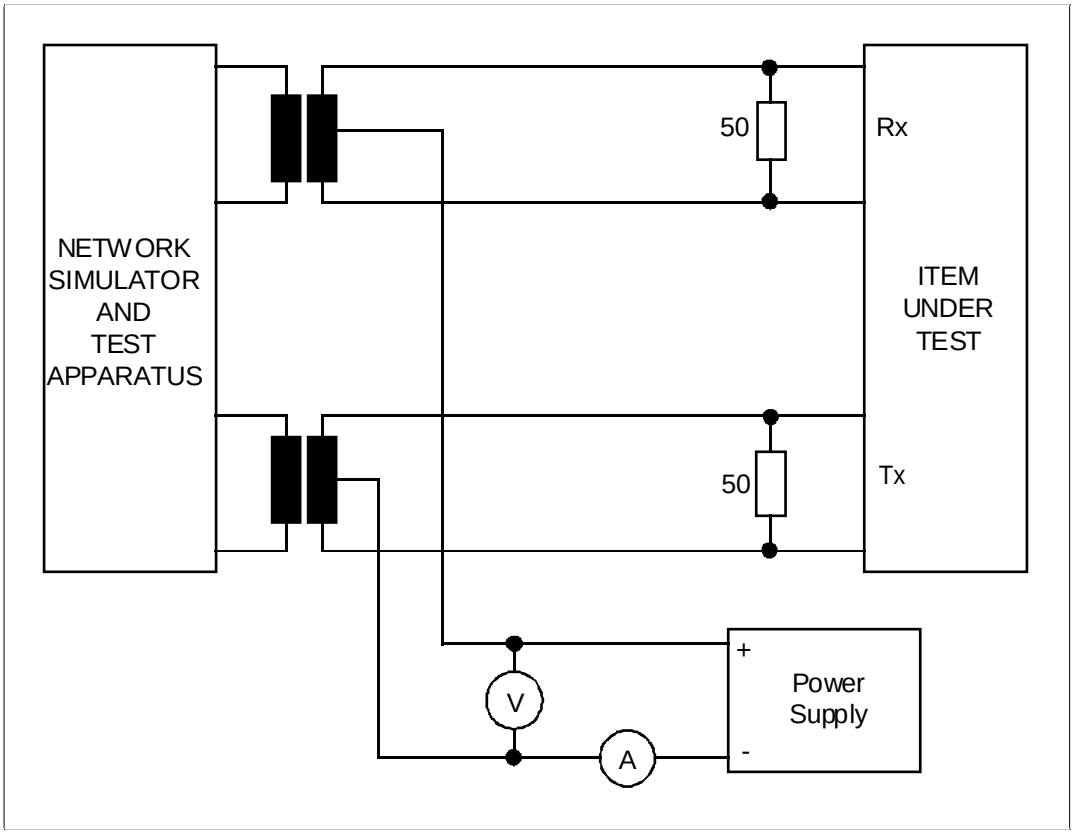
Results: There shall be no power consumed by the TE at both extremes of the power source voltage as stated in the stimulus section *(see NOTE 4 in Clause D.5).*

D.5.1.2 Restricted power conditions (subclause A.9.3.1.2, ETS 300 012)

D.5.1.2.1 Restricted power provision (Test A)

Purpose: To ensure an ACTIVATED designated TE does not consume excessive power from PS1.

Test configuration:



System state: Activated *(state F7)*.

Stimulus: Phantom restricted mode Power Source 1 in the voltage range 40 V, + 5 %/ - 20 % *(42 V to 32 V), (voltage reversal)*.

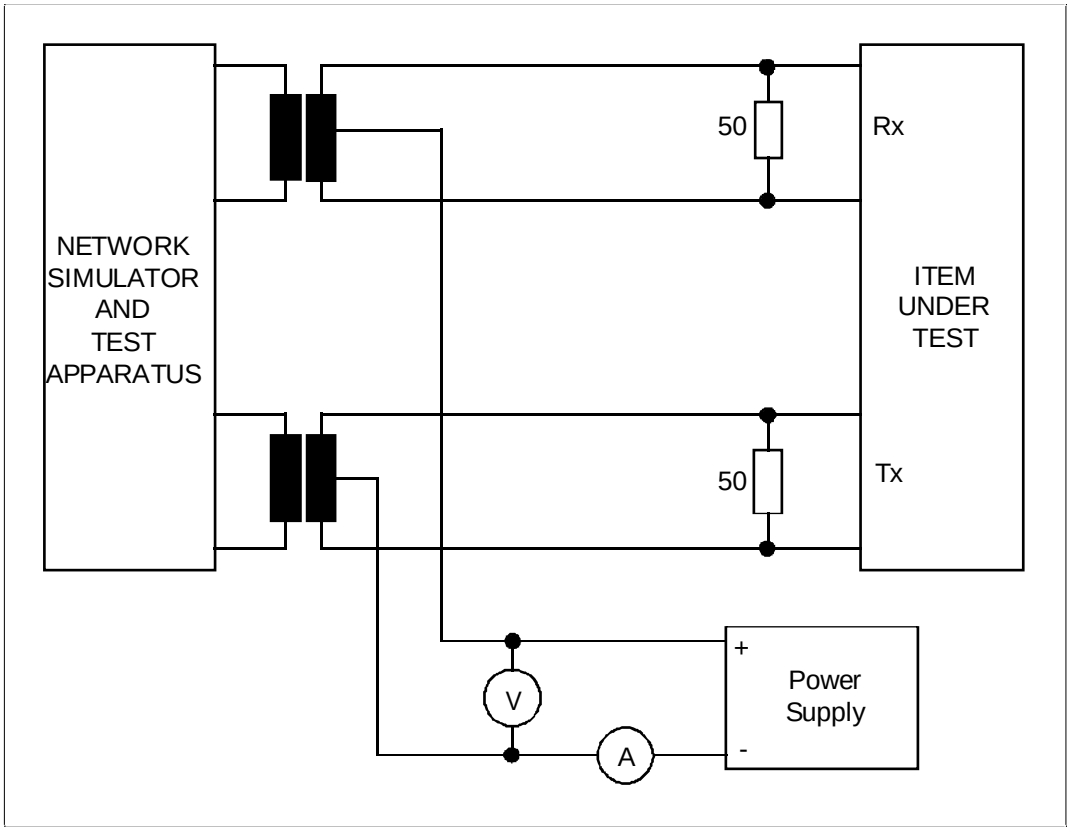
Monitor: DC voltage and current.

Results: The power consumed by the designated TE shall not exceed 380 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.2.2 Restricted power provision (Test B)

Purpose: To ensure a DEACTIVATED designated TE does not consume excessive power from PS1.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Phantom restricted mode Power Source 1 in the voltage range 40 V, + 5 %/- 20 % *(42 V to 32 V), (voltage reversal)*.

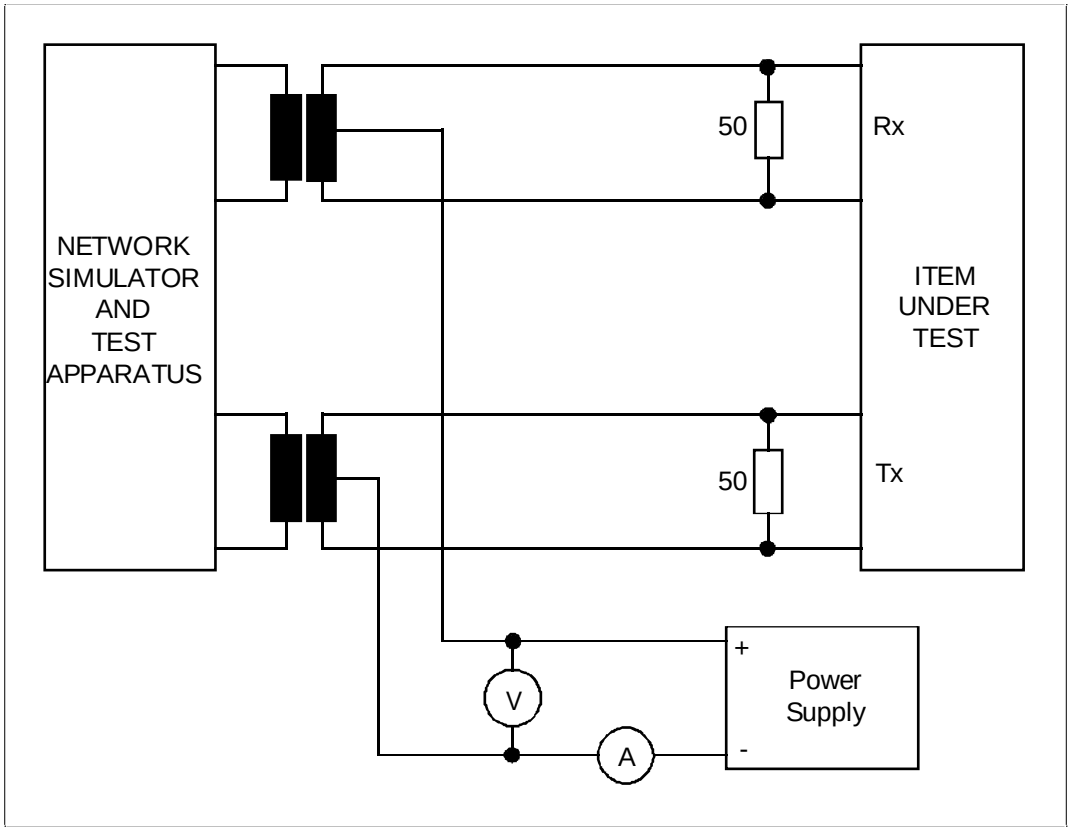
Monitor: DC voltage and current.

Results: The power consumed by the designated TE whilst deactivated shall not exceed 25 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.2.3 Restricted power provision (Test C)

Purpose: To ensure a DEACTIVATED designated TE does not consume excessive power from PS1 during a local action.

Test configuration:



System state: Deactivated *(state F3)*.

Stimulus: Local action. Phantom restricted mode Power Source 1 in the voltage range 40 V, + 5 %/- 20 % *(42 V to 32 V), (voltage reversal)*.

Monitor: DC voltage and current.

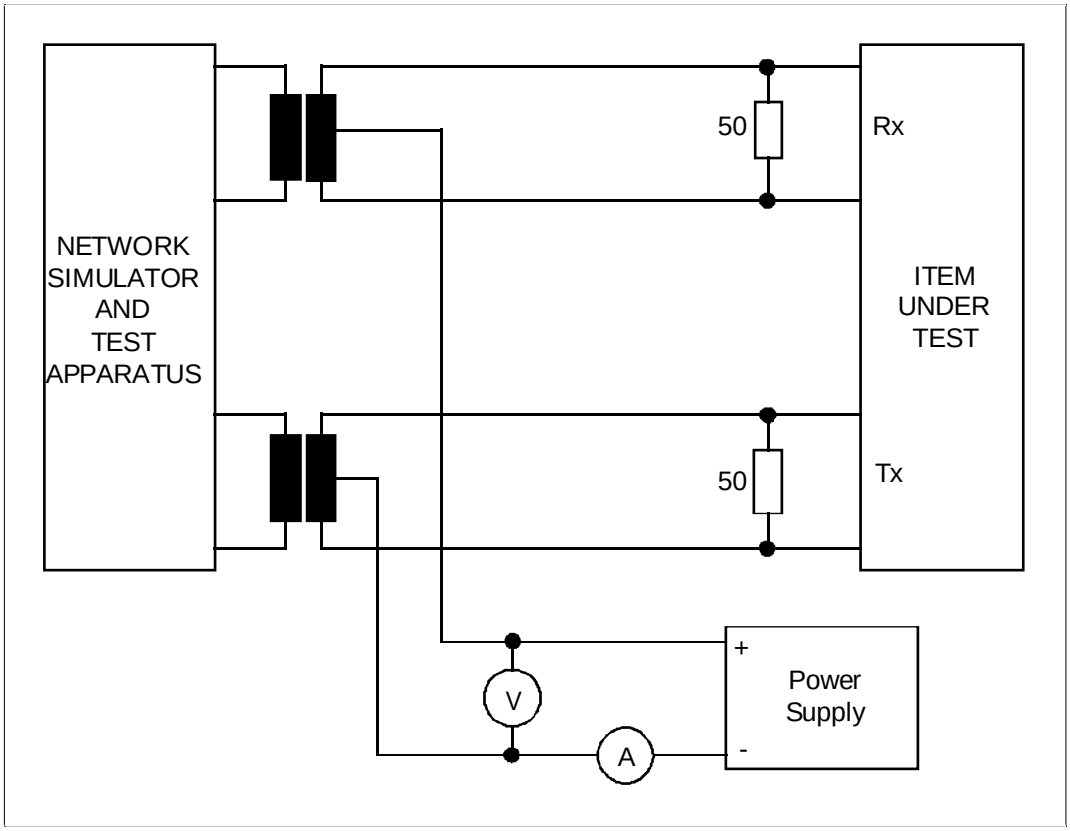
Results: The power consumed by the designated TE shall not exceed 380 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.2.4 Restricted power provision (Test D)

Purpose: To ensure that a locally powered TE, in any state using a connection detector, does not consume excessive power from PS1 (restricted).

NOTE: This requirement also applies to the APS.

Test configuration:



System state: Any state.

Stimulus: Phantom restricted mode Power Source 1 in the voltage range 40 V,+ 5 %/- 20 % *(42 V to 32 V), (voltage reversal)*.

Monitor: DC voltage and current.

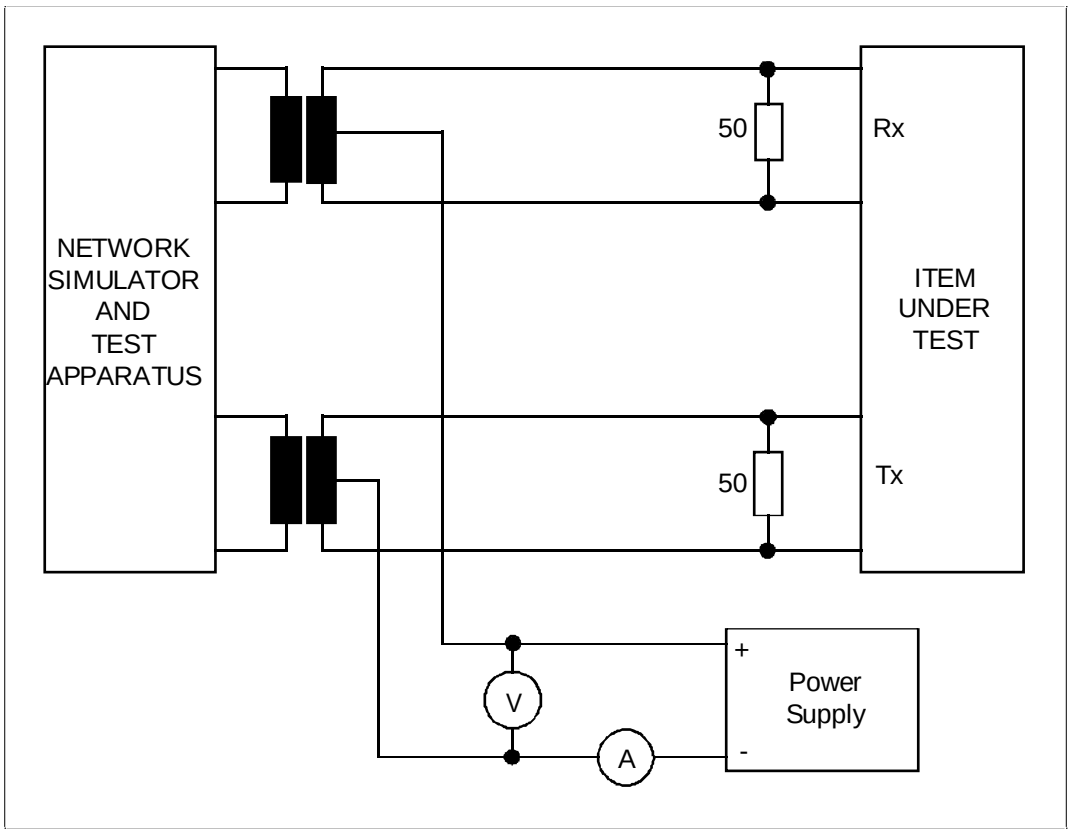
Results: The power consumed by the TE shall not exceed 3 mW at both extremes of the power source voltage as stated in the stimulus section.

D.5.1.2.5 Restricted power provision (Test E)

Purpose: To ensure a LOCALLY POWERED TE not using a connected detector does not consume power from PS1 in any state.

NOTE: This requirement also applies to the APS.

Test configuration:



System state: Any state.

Stimulus: Phantom restricted mode Power Source 1 in the voltage range 40 V, + 5 %/- 20 % *(42 V to 32 V), (voltage reversal)*.

Monitor: DC voltage and current.

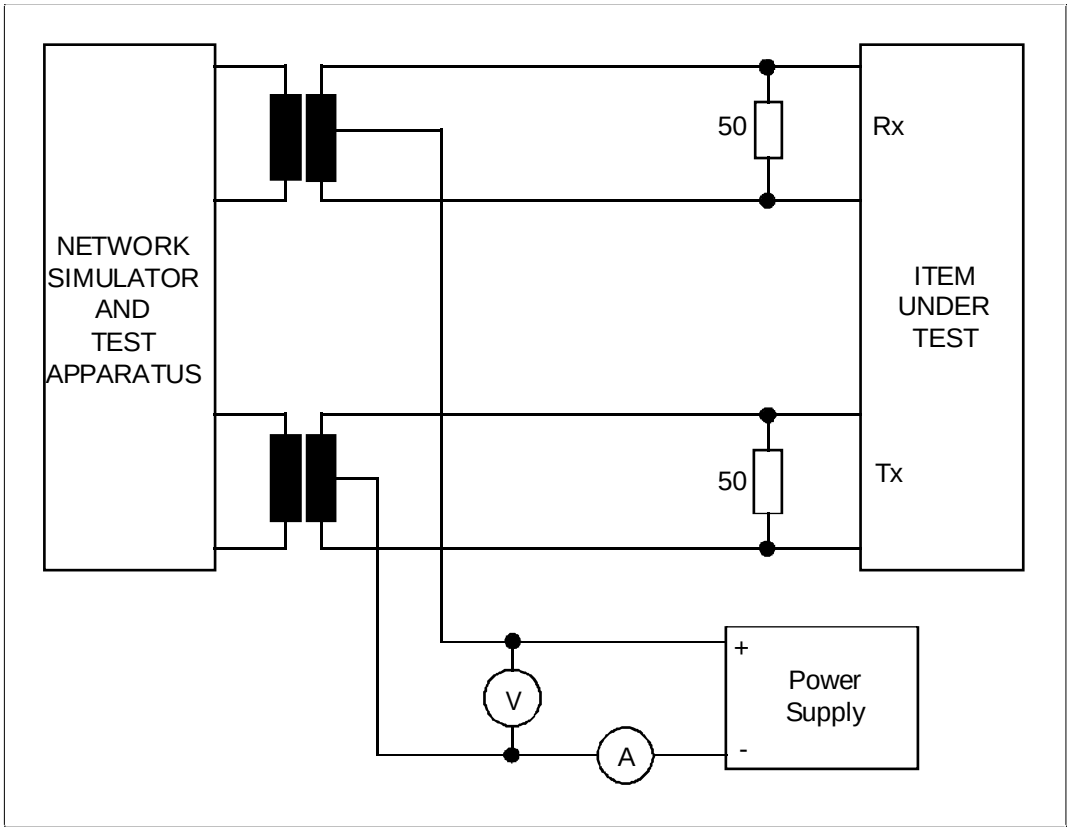
Results: There shall be no power consumed by the TE at both extremes of the power source voltage as stated in the stimulus section *(see NOTE 4, in Clause D.5)*.

D.5.1.2.6 Restricted power provision (Test F)

Purpose: To ensure a non designated TE does not consume excessive power from PS1 in any state.

NOTE: This requirement also applies to the APS.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Phantom restricted mode Power Source 1 in the voltage range 40 V, + 5 %/- 20 % *(42 V to 32 V), (voltage reversal)*.

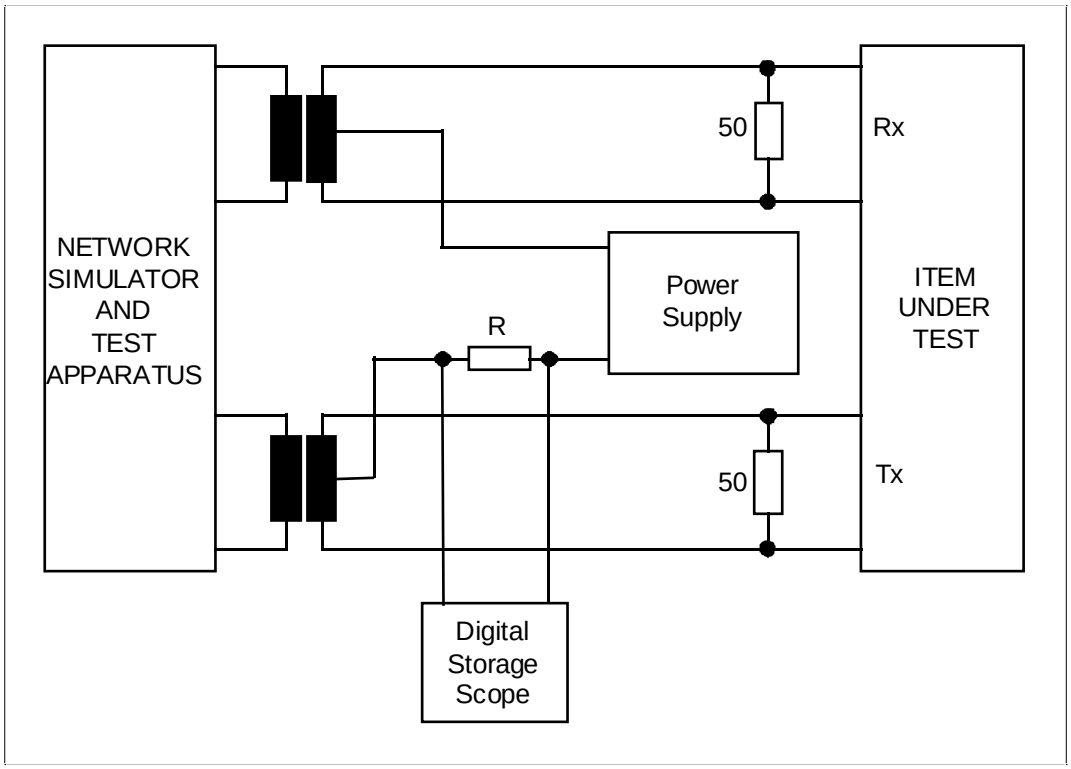
Monitor: DC voltage and current.

Results: There shall be no power consumed by the TE at both extremes of the power voltage as stated in the stimulus section *(see NOTE 4 in Clause D.5).*

D.5.1.3 Current transient (subclause A.9.4, ETS 300 012)

Purpose: To test the rate of change of the current drawn by a TE when the TE is varying its power consumption. This may be caused by changing the state, by some local actions or by some TE typical services.

Test configuration:



System state: Any state from F3 to F8 in normal and restricted mode.

Stimulus: It is dependent on the kind of TE how maximum current can be drawn.

Monitor: Current drawn by the TE.

Results: The current transient shall not exceed 5 mA/µs in the specified voltage range. The slope is measured from 10 % to 90 % of the current change.

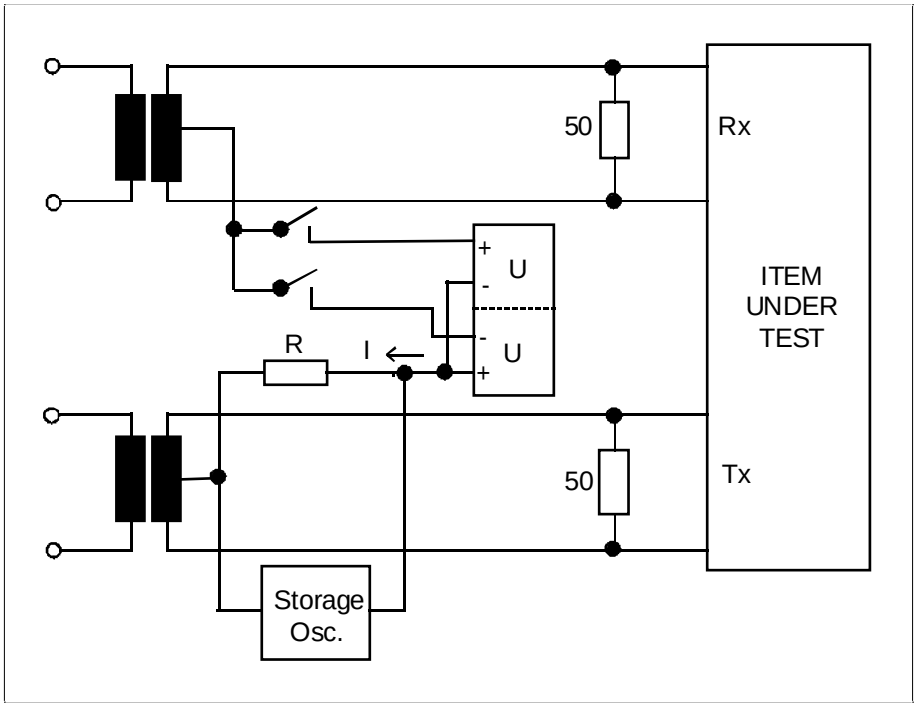
NOTE: To ensure that the measured current transient is not due to a superimposed noise, only a change of current greater than 1,5 mA should be taken into consideration.

D.5.1.4 Limitation on power sink during transient conditions (subclause 7.1, ETS 300 012)

D.5.1.4.1 Current/time limitation for TE (subclause 7.1.1, ETS 300 012)

Purpose: To test the behaviour of current over time when connecting to PS1 in normal and restricted mode.

Test configuration:



NOTE: Ideal switch on condition *(risetime -> 0)*.

System state: Inactive *(state F1)*.

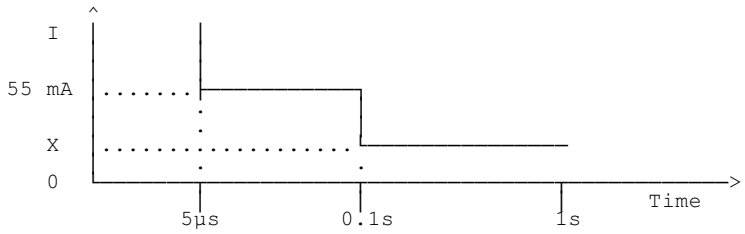
Stimulus: Phantom supply voltage.
- test 1 ... normal mode U = + 40 V R = 15 Ω
- test 2 ... restricted mode

Monitor: Current I over time.

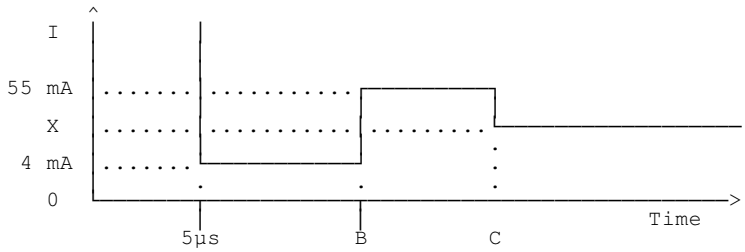
NOTE: The time ZERO is defined when the current detected exceeds 4 mA for the first time.

Results:

a) Current time shall comply with the mask defined in figure 2/subclause 7.1, ETS 300 012 *(time extension to 1s for test of power consumption in t > 100 ms).*



b) For TEs designed to minimise power disturbance *(second alternative described in Annex C of ETS 300 012)*, the current time shall comply with the mask defined in figure 4/ETS 300 012.



5µs ≤ B ≤ 900 ms
C = B + 100 ms

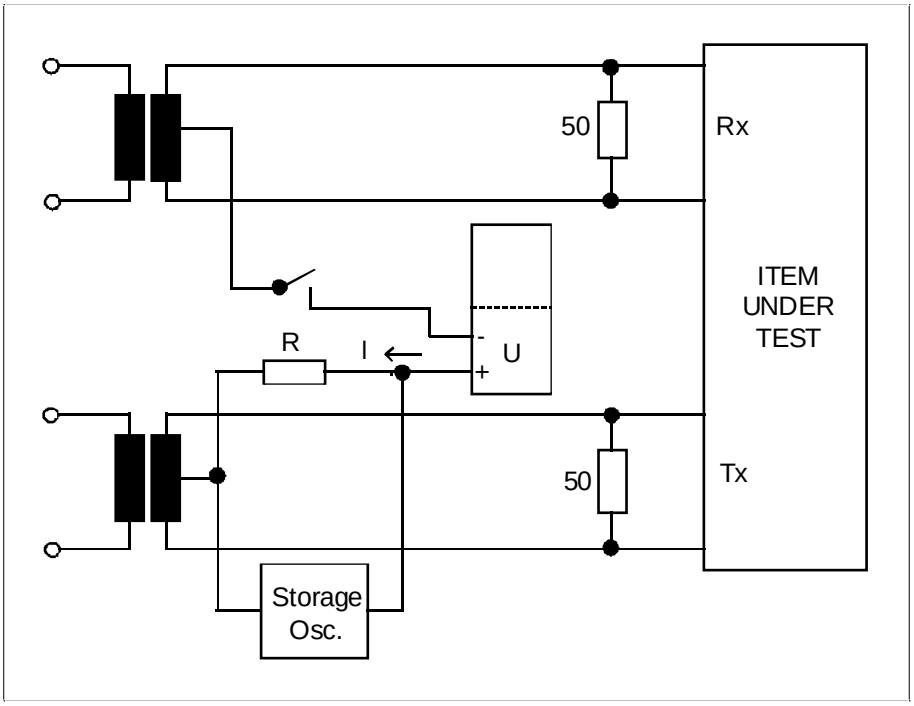
For both cases a and b:

Test 1: X = current equivalent to 1 Watt never exceeding 55 mA independent of the input voltage.
Test 2: X = current equivalent to 380 mW never exceeding 55 mA independent of the input voltage.

D.5.1.4.2 Current/time limitation for TE when connecting (subclause 7.1.1, ETS 300 012)

Purpose: To test the sink current of a non-designated or local powered TE from the phantom in restricted mode when connecting to the S-Bus.

Test configuration:



NOTE: Ideal switch on condition *(risetime -> 0)*.

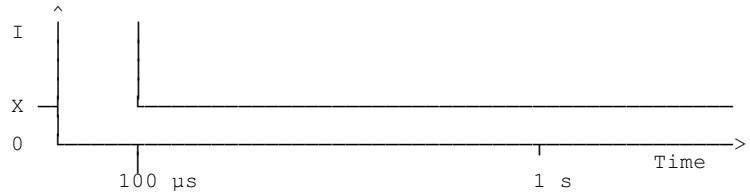
System state: Inactive *(state F1)*.

Stimulus: Phantom supply voltage.Restricted mode
U = - 40 V R = 15 Ω

Monitor: Current I over time.

Results:

Current timing shall comply with the following mask defined in subclause 7.1.1 of ETS 300 012 :

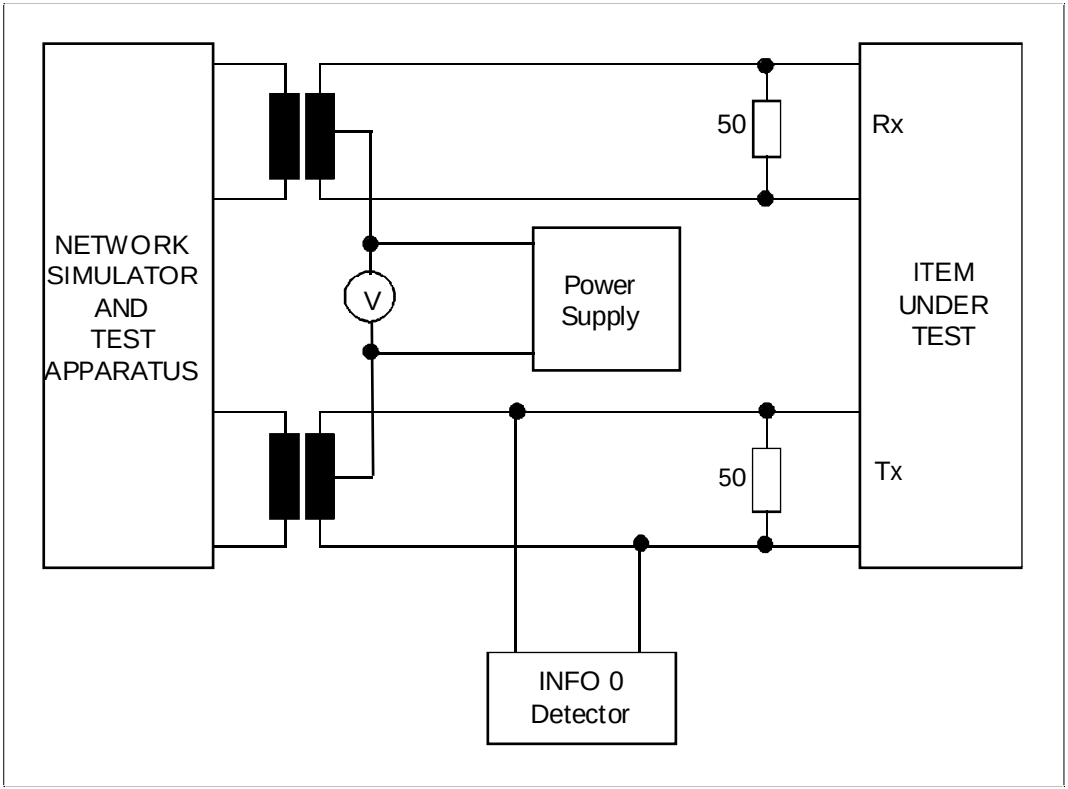


NOTE: a) For TE with connection detector ... X = equivalent 3 mW ;
b) For TE without connection detector ... X = 10 µA.

D.5.1.4.3 Behaviour of a TE using a connection detector (subclause 7.1.1, ETS 300 012)

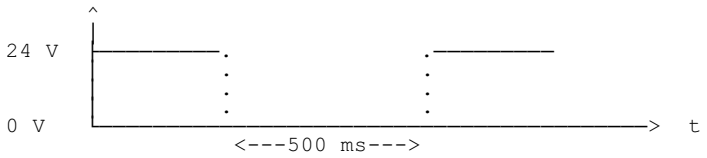
Purpose: To test the connection detector when disconnecting.

Test configuration:



System state: State F4, F6 and F7 in normal and restricted modes.

Stimulus: The PS1 voltage shall be reduced from 24 V to 0 V and then, after 500 ms at 0 V, shall rise again 24 V. The rise and fall time shall each be less than 1 ms.



Monitor: TE transmission line.

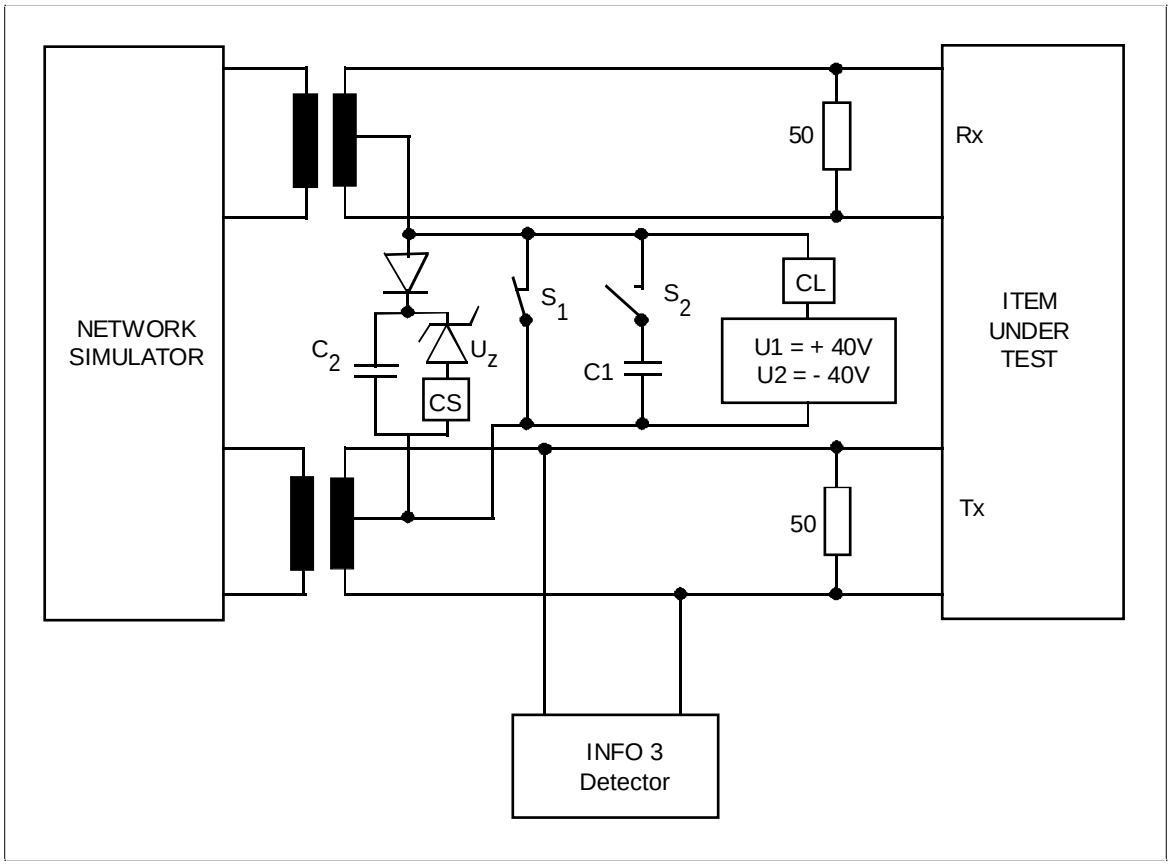
Results: INFO 0 shall not occur.

D.5.1.4.4 Power start-up test (subclause 7.1.3.1, ETS 300 012)

D.5.1.4.4.1 Power start-up test after removal of short-circuit (subclause 7.1.3.1, ETS 300 012)

Purpose: To test the behaviour of TE input voltage over time after removal of short-circuit.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Removal of short-circuit and NT sending INFO 2.

Test 1: Restricted mode.
Test parameters (see table 4, ETS 300 012).
Test 2: Normal mode.
Test parameters (see table 5, ETS 300 012).

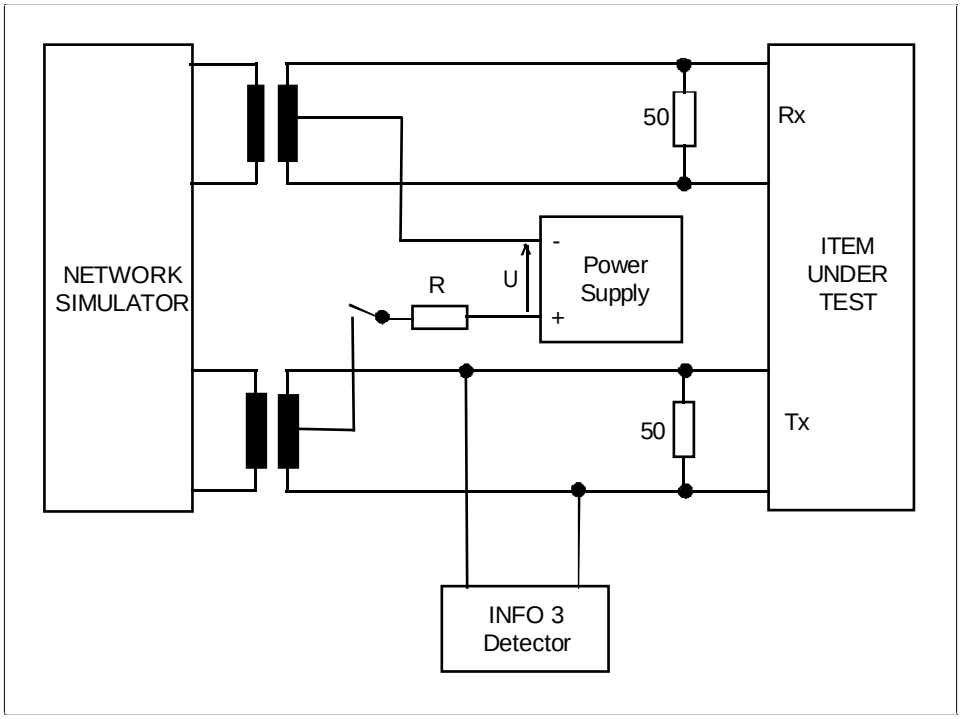
Monitor: Transmission of INFO 3 *(TE -> Network Simulator)*.

Results: TE shall transmit INFO 3 after removal of short-circuit.

D.5.1.4.4.2 Power start-up test at low input voltage (subclause 7.1.3.1, ETS 300 012)

Purpose: To test the power start-up of a TE when connected to Power Source 1 normal at low voltage.

Test configuration:



System state: Inactive *(state F1)*.

Stimulus: Phantom supply voltage *(normal mode)* and INFO 2.
U = 28 V.
R = 70 Ω.

Monitor: Transmitted line signal.

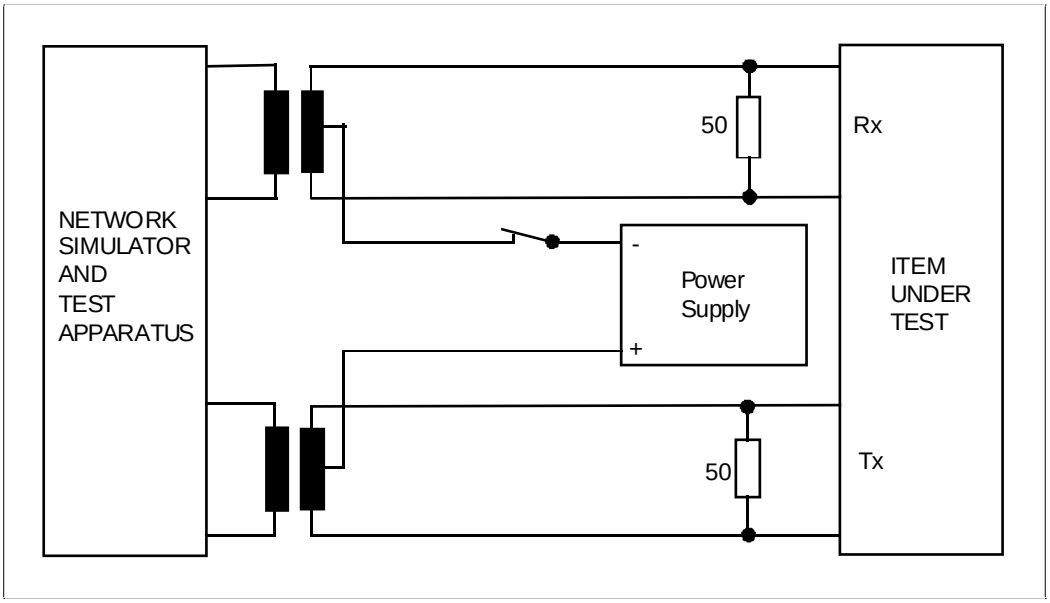
Result: TE shall transmit INFO 3 after the switch-on of the power source.

D.5.1.4.5 Protection against short-term interruptions (subclause 7.1.3.2, ETS 300 012)

D.5.1.4.5.1 Normal power

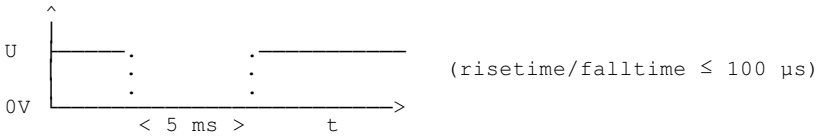
Purpose: To ensure that an IUT does not lose an ongoing communication when the provision of power in normal power mode is interrupted.

Test configuration:



System state: Activated *(state F7)* with maximum power consumption and communication established.

Stimulus: Normal mode U = 24 V.



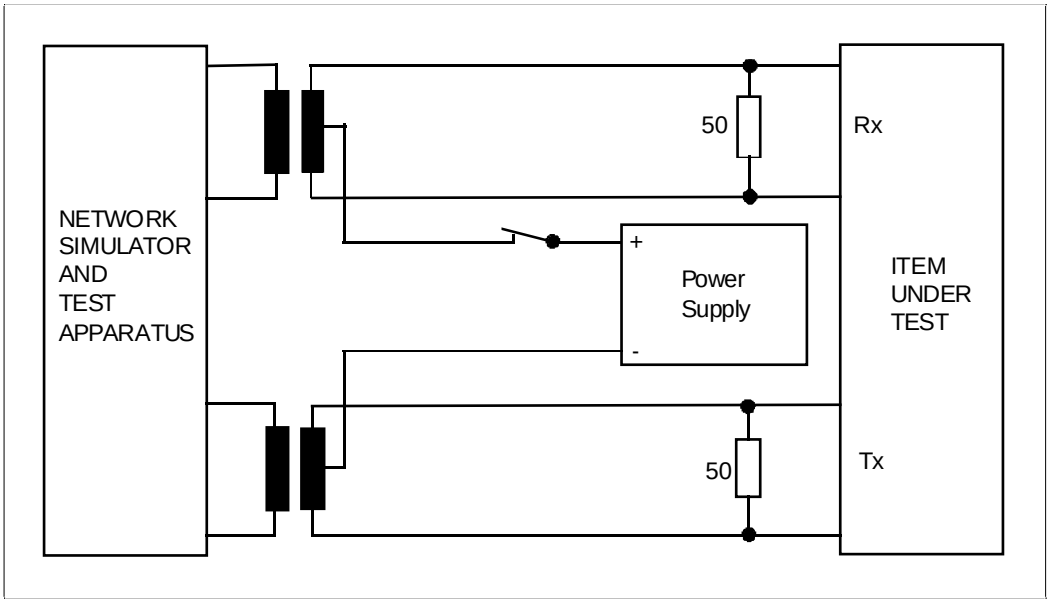
Monitor: Ongoing communication.

Results: No loss of ongoing communication.

D.5.1.4.5.2 Restricted power

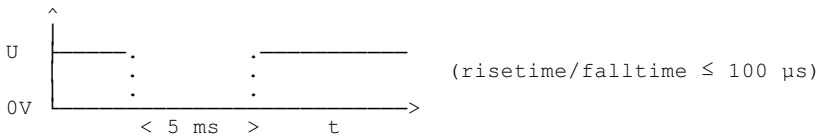
Purpose: To ensure that a IUT does not lose an ongoing communication when the provision of power in restricted power mode is interrupted.

Test configuration:



System state: Activated *(state F7)* with maximum power consumption and communication established.

Stimulus: Restricted mode U = 32 V, Power Source 1.



Monitor: Ongoing communication.

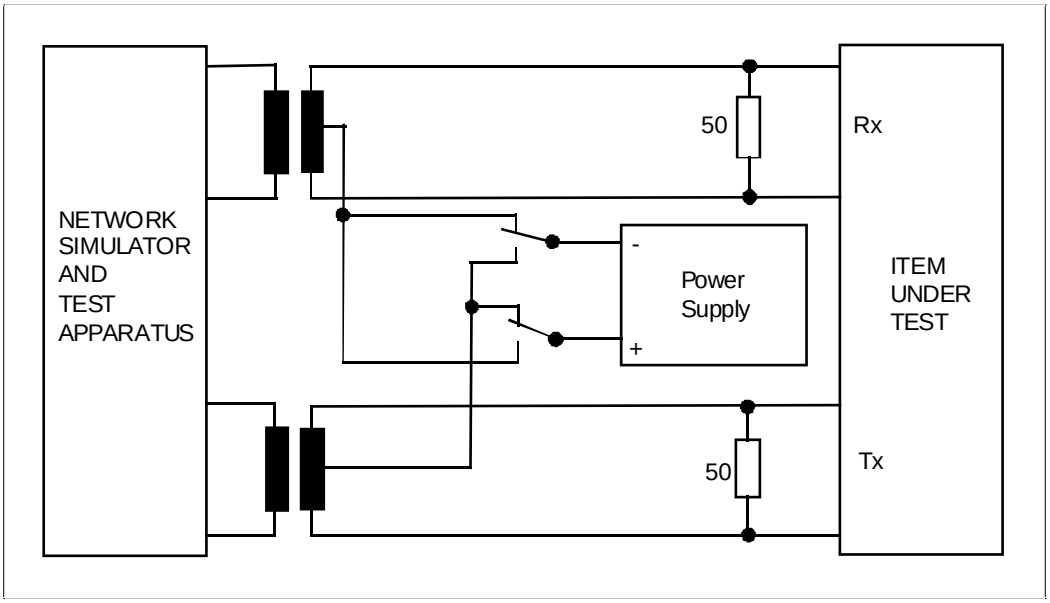
Results: No loss of ongoing communication.

D.5.1.4.6 Behaviour at the switch-over (subclause 7.1.3.3-ETS 300 012)

D.5.1.4.6.1 Normal power

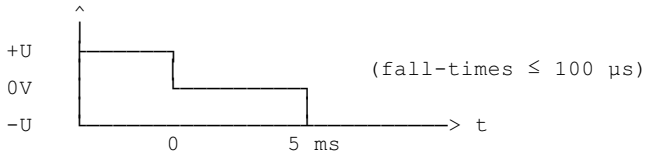
Purpose: To check the reaction of an IUT under normal power condition, when the mode changes from normal to restricted mode.

Test configuration:



System state: Activated *(state F7)* with maximum power consumption.

Stimulus: Change from + 32 V without current limitation to - 40 V with 11 mA current limitation.



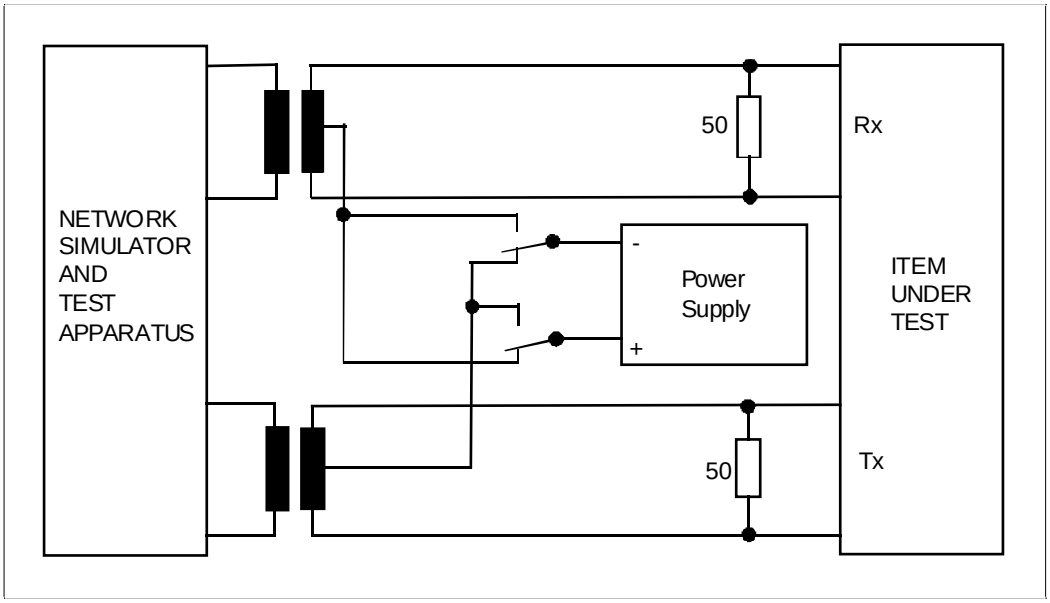
Monitor: Ongoing communication.

Results: No loss of the ongoing communication.

D.5.1.4.6.2 Restricted power (subclause 7.1.3.3, ETS 300 012)

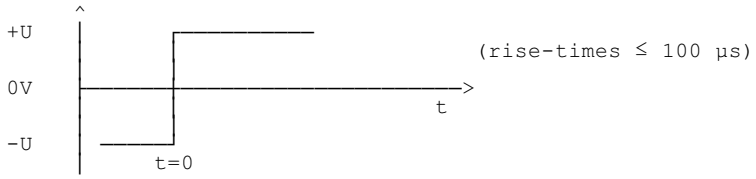
Purpose: To check the reaction of power consumption of an IUT after change from restricted to normal mode.

Test configuration:



System state: Activated *(state F7)* with maximum power consumption.

Stimulus: Change from restricted mode *(U = - 32 V)* to normal mode *(U = + 32 V)*.



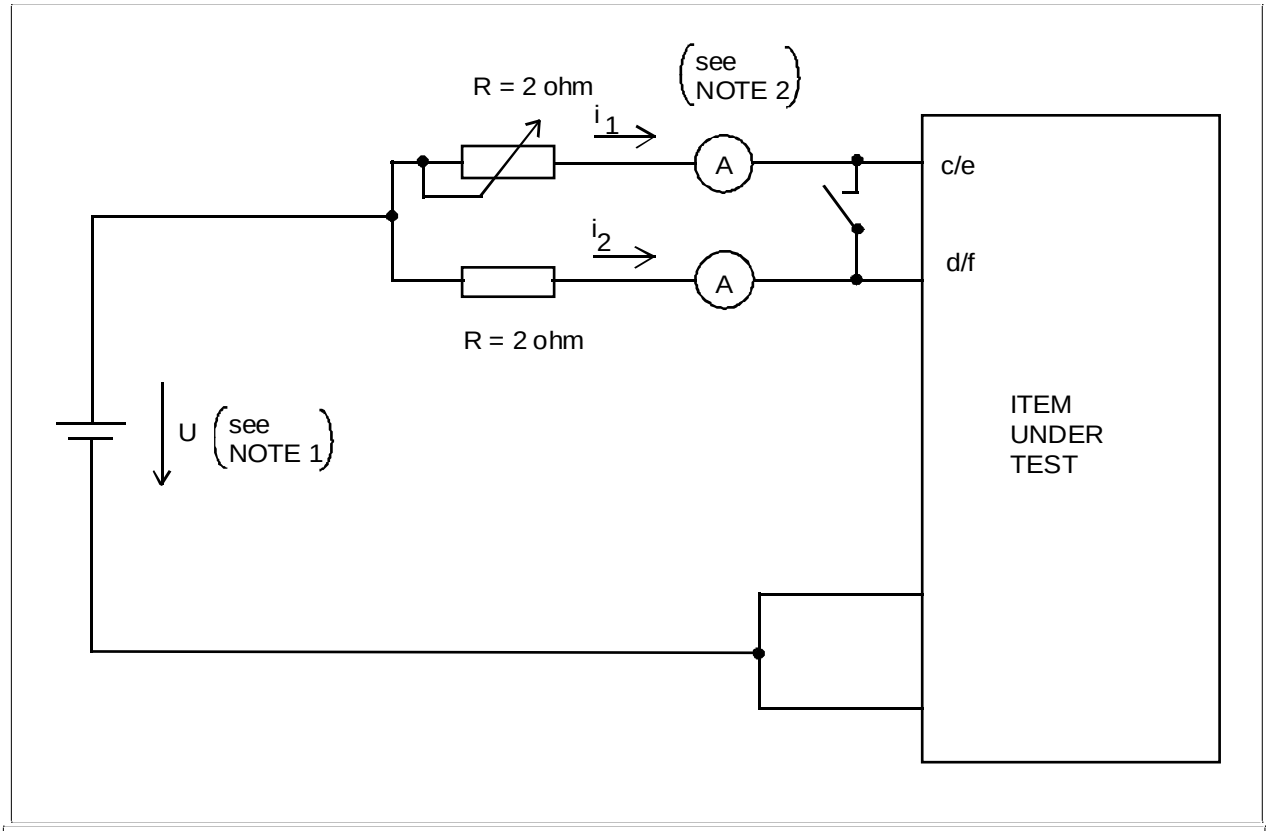
Monitor: DC-voltage and DC-current.

Results: The IUT shall not draw more than 380 mW from 0 < t < 500 ms.

D.5.1.4.7 DC unbalance of TEs using power sink 1 (subclause 7.2.1.2, ETS 300 012)

Purpose: To test the DC unbalance of the receiver and transmitter circuit.

Test configuration:



NOTE 1: The polarity of U (and i) is represented for testing the transmitter side (c and d) wires); for testing the receiver (e and f wires), the polarity shall be reversed.

NOTE 2: Before connecting IUT, calibration to get the same current in both wires shall be done.

System state: Deactivated *(state F3)*.

Monitor: The currents i1 and i2 at the receiver and transmitter sides.

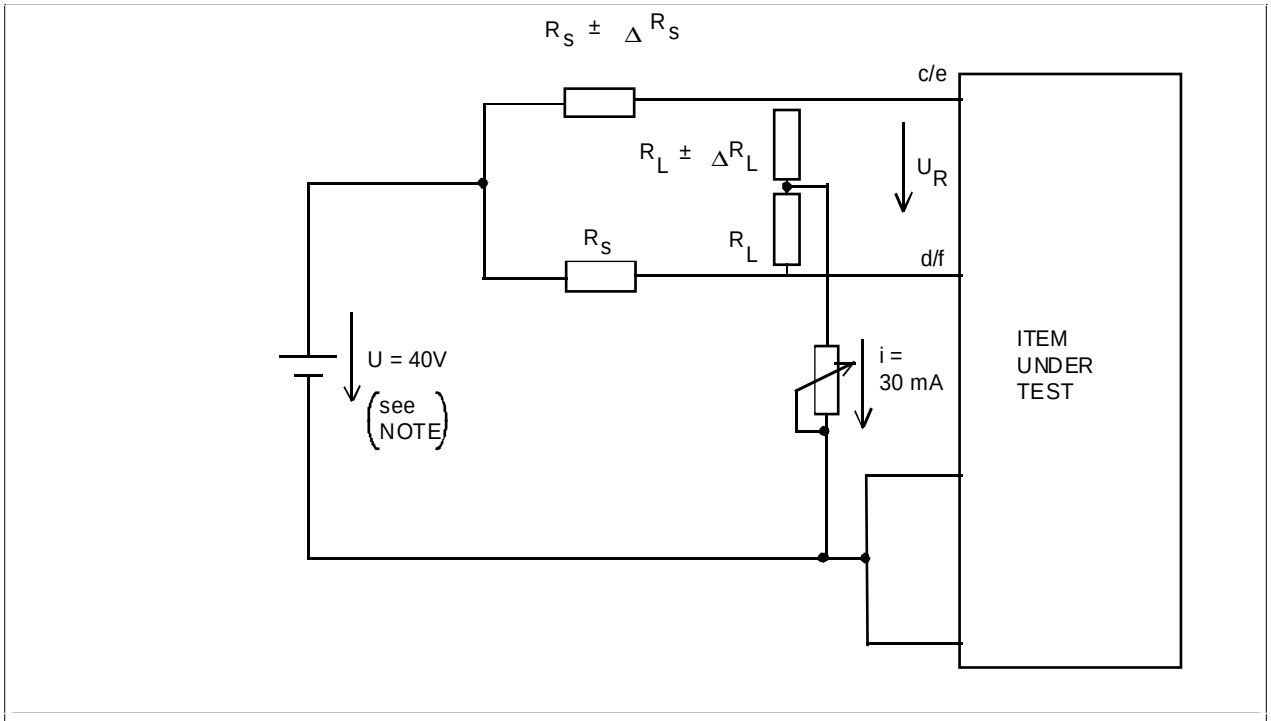
Results: The direct current unbalance *(X)* shall be less than 3 %.

$$X[\%] = \frac{|i1 - i2|}{i1 + i2} * 100$$

D.5.1.4.8 Effect of current unbalance (subclause 7.2.2, ETS 300 012)

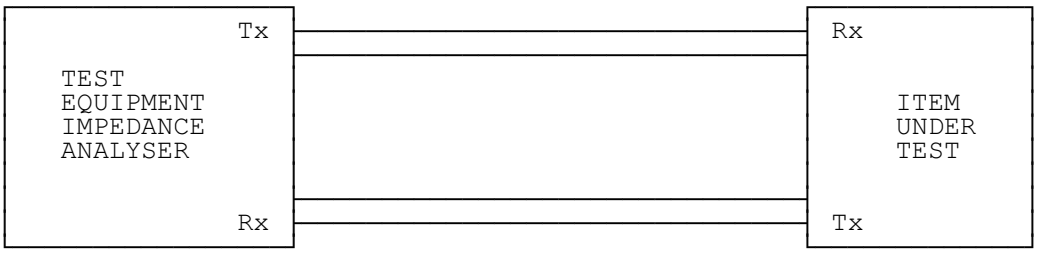
Purpose: To test the impedance of the receiver and transmitter when a direct current unbalance is applied.

Test configuration 1:



NOTE: The polarity of U is represented for testing the transmitter side (c and d wires) for testing the receiver (e and f wires), the polarity must be reversed.

Test configuration 2:



System state: Deactivated *(state F3)*.

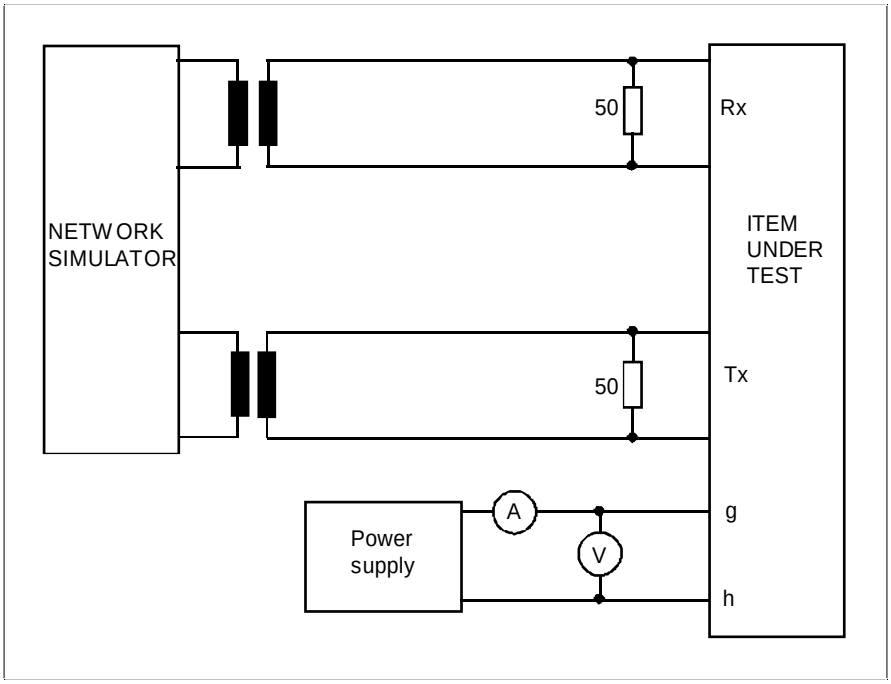
Stimulus:

Test configuration 1 :	Power source 1 normal with test circuit applied with both polarities at the receiver and transmitter side.
Test configuration 2:	Sinusoidal voltage of 100 mV rms, in the frequency range of 2 kHz to 20 kHz, superimposed with the DC voltage UR as measured in test configuration 1.
Monitor:	DC voltage at c to d and e to f at both polarities. For both transmitter and receiver, the greater value is taken for the next step as specified in test configuration 2.
	Impedance.
Results:	Shall exceed the impedance template as given in figure 12/I.430 [2] in the range from 2 kHz to 20 kHz.

D.5.2 Power Source 2 - Optional third pair (subclause A.9.3.2, ETS 300 012)

Purpose: To ensure a TE does not draw excessive power from a Power Source 2 whilst in any state.

Test configuration:



System state: Any state.

Stimulus: Power Source 2 in the voltage range 40 V, + 5 % / - 20 % *(42 V to 32 V)*.

Results: The power drawn *(V * I)* shall not exceed N Watt at both extremes of the power source voltage as stated in the stimulus section.

a) normal power conditions : N = 7 Watts
b) restricted power conditions : N = 2 Watts

Annex E (normative): Conformance test principles to interface point I_b

E.1 Scope and general information

E.1.1 Scope

This annex provides the test principles for the requirements of this ETS used to determine the compliance of an Item Under Test (IUT) to this ETS.

It is outside the scope of this annex to identify the specific tests required by an implementation where equipment has to meet attachment approval.

Detailed test equipment accuracy and the specific tolerance of the test devices is not a subject of this annex.

In the case where an PTNX does not use a connection cord at the S reference point, the location of interface I_b shall be declared by the PTNX supplier.

The test configurations given do not imply a specific realisation of test equipment or arrangement or the use of specific test devices for conformance testing. However any test configuration used shall provide those test conditions specified under "system state", "stimulus" and "monitor" for each individual test *(the measurement arrangements and the equipment suggested are only for example purposes)*.

Unless otherwise stated, the conformance tests described in the present document do not apply to the Auxiliary Power Supply *(APS)*.

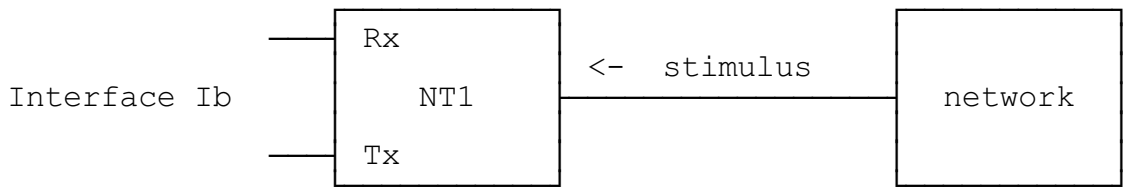
E.1.2 General information

Normally, an equipment providing an interface I_b of the basic rate access cannot be tested by applying a stimulus only at this interface *(see the figures below)*. For some tests, a signal providing the timing clock must be applied to the "master" interface of such an equipment. If necessary, this signal must contain the INFOs used to bring the IUT in the defined system states. Examples for a "master" interface where the IUT is synchronised are :

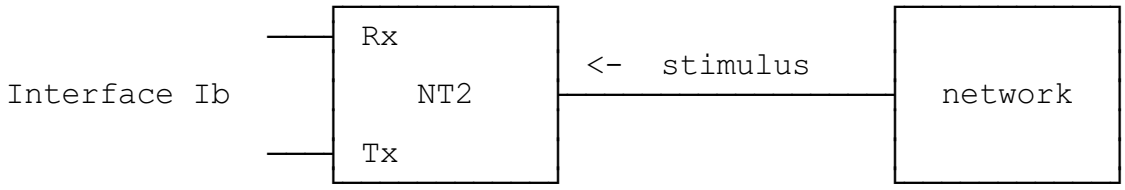
- any U interface in case of a NT1;
- a basic or primary rate access in case of a NT2.

Only when a NT2 is not synchronised, it can be tested separately.

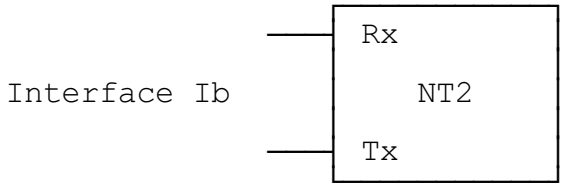
A description of the signals applied to the "master" interface or of the action to the user shell of an IUT are outside the scope of these test principles.



NT1 is synchronised to a network.



NT2 is synchronised to a network.



NT2 is not synchronised to a network *(free running mode)*.

For conformance test purposes, it is required that the terminating resistors *(100 Ω)* shall be removed from the NT receiving and transmitting pairs *(It is sufficient to remove the terminating resistors only in the equipment provided for conformance test purposes)*. In this case the value of the resistors shall be checked *(100 Ω ± 5 %)* and the NT with its installed terminating resistors shall also conform to this ETS.

IUT suppliers shall provide information on how IUT primitive exchanges can be detected i.e. primitives activate, deactivate, management primitives between layer 1 and high layers.

Ideal values for components and circuits are considered in the test principles.

Unless otherwise stated the line termination resistors for both NT and TE sides are considered inside the test equipment.

E.1.3 Definitions and abbreviations

For the purpose of this annex the following definitions and abbreviations together with those given in Clause 3 apply:

- IUT *(Item Under Test)*

  Interface point I_b i.e. NT2 or access connection element *(see also I.430 [2]/Annex E.1 definition 109)*.

- Rx *(Receiver)*

  Interface signal receiver of IUT or simulator.

- Tx *(Transmitter)*

  Interface signal transmitter of IUT or simulator.

- Simulator

  Device generating the stimulus signal for the IUT and monitoring the signal transmitted by the IUT to test the characteristics of NT.

E.1.4 Allocation of tests

E.1.4.1 General

General	Clause/ Subclause	Test defined in Clause/subclause
General	A.1	N/R 1)

1) N/R: not relevant

E.1.4.2 Service characteristics

Services	Clause/ Subclause	Test defined in Clause/subclause
Service characteristics	A.2	N/R
Services required	A.2.1	N/R
Services to Layer 2	A.2.2	N/R
Transmission capability	A.2.2.1	N/R
act/deact	A.2.2.2	N/R
D-channel access	A.2.2.3	N/R
Maintenance	A.2.2.4	N/R
status indication	A.2.2.5	N/R
primitive	A.2.3	N/R

E.1.4.3 Modes of operation

Modes	Clause/ Subclause	Test defined in Clause/subclause
Modes of operation	A.3	N/R
Point to point	A.3.1	N/R
Point to Multipoint	A.3.2	N/R

E.1.4.4 Wiring

Modes	Clause/ Subclause	Test defined in Clause/subclause
Types of wiring configuration	A.4	N/R
Point-to-point configuration	A.4.1	N/R
Point-to-multipoint config.	A.4.2	N/R
Polarity Integrity (figure 2-I.430 [2])	A.4.3	N/R
Interface Ib	A.4.4	N/R
NT associated wiring	A.4.5	N/R

E.1.4.5 Functional characteristics

Functions	Clause/ Subclause	Test defined in Clause/subclause
Functional characteristics	A.5	N/R
Interface functions	A.5.1	N/R
B-channel	A.5.1.1	E.2.1
Bit timing	A.5.1.2	E.2.1.1
Octet timing	A.5.1.3	E.2.1
Frame alignment	A.5.1.4	E.3.4
D-channel	A.5.1.5	E.2.1.1
D-channel access procedure	A.5.1.6	E.3.2
Power feeding	A.5.1.7	E.5
Deactivation	A.5.1.8	E.3.3
Activation	A.5.1.9	E.3.3
Interchange circuits	A.5.2	E.2.1
Connect/disconnect indication	A.5.3	N/R
TE powered across interface	A.5.3.1	N/R
TE not powered across interface	A.5.3.2	N/R
Indication of connection status	A.5.3.3	N/R
Frame structure	A.5.4	E.2.1
Bit rate	A.5.4.1	E.2.1.1
Binary organisation of the frame	A.5.4.2	N/R
TE to NT	A.5.4.2.1	N/R
NT to TE	A.5.4.2.2	E.2.1
Relative bit positions	A.5.4.2.3	E.2.1.1
Line Code	A.5.5	E.2.1.1
Timing considerations	A.5.6	E.2.1.1

E.1.4.6 Interface procedures

Procedure = D-channel Access	Clause/ Subclause	Test defined in Clause/subclause
Interface procedures	A.6	N/R
D-channel Access procedure	A.6.1	N/R
Interframe (Layer 2) timefill	A.6.1.1	E.3.1
D-echo channel	A.6.1.2	E.3.2
D-channel monitoring	A.6.1.3	N/R
Priority mechanisms	A.6.1.4	N/R
Collision detection	A.6.1.5	N/R
Priority system	A.6.1.6	N/R

Procedure = Act/Deactivation	Clause/ Subclause	Test defined in Clause/subclause
Activation/Deactivation	A.6	N/R
Definitions	A.6.2.1	N/R
TE states	A.6.2.1.1	N/R
F1	A.6.2.1.1.1	N/R
F2	A.6.2.1.1.2	N/R
F3	A.6.2.1.1.3	N/R
F4	A.6.2.1.1.4	N/R
F5	A.6.2.1.1.5	N/R
F6	A.6.2.1.1.6	N/R
F7	A.6.2.1.1.7	N/R
F8	A.6.2.1.1.8	N/R
NT states	A.6.2.1.2	N/R
G1	A.6.2.1.2.1	E.3.3.1
G2	A.6.2.1.2.2	E.3.3.1
G3	A.6.2.1.2.3	E.3.3.1
G4	A.6.2.1.2.4	E.3.3.1
Activate primitives	A.6.2.1.3	E.3.3
Deactivation primitives	A.6.2.1.4	E.3.3
Management primitives	A.6.2.1.5	E.3.3
Valid primitive sequences	A.6.2.1.6	N/R
Signals	A.6.2.2	E.2.1.1, E.2.1.2
TE activation procedures	A.6.2.3	E.3.3.1
General TE procedures	A.6.2.3.1	N/R
Specification of procedure	A.6.2.3.2	N/R
Act/Deactivation on network side	A.6.2.4	N/R
Activating/Deactivating NT	A.6.2.4.1	E.3.3
Non activating/non deactivating	A.6.2.4.2	E.3.3
Timer values	A.6.2.5	E.3.3.2.3
Activation time	A.6.2.6	N/R
TE activation times	A.6.2.6.1	N/R
NT activation times	A.6.2.6.2	E.3.3.2.1, E.3.3.2.2
Deactivation time	A.6.2.7	E.3.3.2.2

Procedure = Frame Alignment	Clause Subclause	Test defined in Clause/subclause
Frame alignment procedures	A.6.3	E.3.4
Frame alignment NT to TE	A.6.3.1	N/R
Loss of frame alignment	A.6.3.1.1	N/R
Frame alignment	A.6.3.1.2	N/R
Frame alignment TE to NT	A.6.3.2	E.3.4
Loss of frame alignment	A.6.3.2.1	E.3.4
Frame alignment	A.6.3.2.2	E.3.4
Multiframing	A.6.3.3	N/R
B-channel idle code	A.6.4	N/R

E.1.4.7 Maintenance

Functions	Clause/ Subclause	Test defined in Clause/subclause
Layer 1 maintenance	A.7	N/R

E.1.4.8 Electrical characteristics

Functions	Clause/ Subclause	Test defined in Clause/subclause
Electrical characteristics	A.8	N/R
Bit rate	A.8.1	E.4.1
Nominal bit rate	A.8.1.1	E.4.1.1, E.4.1.2
Tolerance	A.8.1.2	E.4.1.1, E.4.1.2
Jitter & bit phase	A.8.2	N/R
Test configurations	A.8.2.1	N/R
Timing extraction jitter	A.8.2.2	N/R
Total phase deviation	A.8.2.3	N/R
NT jitter characteristics	A.8.3	E.4.2
Termination of the line	A.8.4	N/R
Transmitter O/P characteristics	A.8.5	N/R
Transmitter output impedance	A.8.5.1	N/R
NT Transmitter output impedance	A.8.5.1.1	E.4.3
TE Transmitter output impedance	A.8.5.1.2	N/R
Test load impedance	A.8.5.2	N/R
Pulse shape and amplitude	A.8.5.3	E.4.4
Pulse shape	A.8.5.3.1	E.4.4
Nominal pulse amplitude	A.8.5.3.2	E.4.4
Pulse unbalance	A.8.5.4	N/R
- pulse amplitude (high density pattern)	A.8.5.4.1	E.4.5.1
- pulse unbalance of an isolated couple of pulses	A.8.5.4.2	E.4.5.2
Voltage on other test loads	A.8.5.5	N/R
400 ohm load	A.8.5.5.1	N/R
5.6 ohm load	A.8.5.5.2	N/R
Unbalance about earth	A.8.5.6	E.4.6
Longitudinal conversion loss	A.8.5.6.1	E.4.6
Output signal balance	A.8.5.6.2	N/R
Receiver Input Characteristics	A.8.6	N/R
Receiver Input Impedance	A.8.6.1	N/R
TE receiver input impedance	A.8.6.1.1	N/R
NT receiver input impedance	A.8.6.1.2	E.4.7.1
Receiver sensitivity (N & DI)	A.8.6.2	E.4.7.2
TEs	A.8.6.2.1	N/R
NTs for short passive bus	A.8.6.2.2	E.4.7.2
NT for pt-pt and short passive	A.8.6.2.3	E.4.7.2
NT for extended passive bus	A.8.6.2.4	E.4.7.2
NT for pt-pt only	A.8.6.2.5	E.4.7.2
NT receiver input delay	A.8.6.3	E.4.7.3
NT for short passive bus	A.8.6.3.1	E.4.7.3
NT for pt-pt and passive bus	A.8.6.3.2	E.4.7.3
NT for extended passive bus	A.8.6.3.3	E.4.7.3
NT for pt-pt only	A.8.6.3.4	E.4.7.3
Unbalance about earth	A.8.6.4	E.4.7.4
Isolation from external voltages	A.8.7	N/R
Interconnect media LCL	A.8.8	N/R
ISDN basic access TE cord	A.8.9	N/R

E.1.4.9 Power feeding

Static requirements	Clause/ Subclause	Test defined in Clause/subclause
Power Feeding	A.9	N/R
Reference configuration	A.9.1	N/R
Functions at the access leads	A.9.1.1	E.2.1.1, E.5.1.1, E.5.1.2
Provision of source and sinks	A.9.1.2	E.5.1.2
Power available from NT	A.9.2	E.5.1.4.1
PS1, normal and restricted	A.9.2.1	E.5.1.1, E.5.1.2, E.5.1.3
Min volts at NT from PS1	A.9.2.2	N/R
Normal condition	A.9.2.2.1	E.5.1.1
Restricted power condition	A.9.2.2.2	E.5.1.2
Min volts of power source 2	A.9.2.3	E.5.2
Power available at TE	A.9.3	N/R
Source 1 - phantom mode	A.9.3.1	N/R
Normal condition	A.9.3.1.1	N/R
Restricted power condition	A.9.3.1.2	N/R
Source 2 - option third pair	A.9.3.2	N/R
Normal condition	A.9.3.2.1	N/R
Restricted power condition	A.9.3.2.2	N/R
Current transient	A.9.4	N/R
Power source 1 consumption	A.9.5	N/R
Normal condition	A.9.5.1	N/R
Restricted power condition	A.9.5.2	N/R
Power available to designated TE	A.9.5.2.1	N/R
Power to non-designated TEs	A.9.5.2.2	N/R
Galvanic Isolation	A.9.6	N/R

Dynamic requirements	Clause / Subclause	Test defined in Clause/subclause
Additional requirements	7	N/R
Limitations on power source and sink during transient conditions	7.1	N/R
Current/time limitations for TEs	7.1.1	N/R
Power source switch-over	7.1.2	N/R
Power source switch-over time	7.1.2.1	E.5.1.3
Restricted mode power source requirements under overload conditions	7.1.2.2	E.5.1.4
Other TE requirements	7.1.3	N/R
Minimum TE start-up current	7.1.3.1	N/R
Protection against short term interruptions	7.1.3.2	N/R
Behaviour at the switch-over	7.1.3.3	N/R
Effective capacitance at the PS1 input	7.1.3.4	N/R
Other power source requirements	7.1.4	N/R
Power Source 1 restricted	7.1.4.1	E.5.1.4.2, E.5.1.4.3 E.5.1.4.4
Power Source 1 normal	7.1.4.2	N/R
Requirements for type a) sources	7.1.4.3	E.5.1.5, E.6.1.3
Requirements for both types of sources	7.1.4.4	N/R
Switch-on surge capability	7.1.4.4.1	E.5.1.6, E.6.1.4
TE connection surge capability	7.1.4.4.2	E.5.1.7, E.6.1.5
Current unbalance	7.2	N/R
Direct current unbalance	7.2.1	N/R
DC unbalance of Power Source 1	7.2.1.1	E.5.1.8
DC unbalance of Power Sink 1	7.2.1.2	N/R
Differential resistance in a pair of the installation wiring	7.2.1.3	N/R
Current unbalance in a pair	7.2.2	E.5.1.9, E.6.1.6

Requirements from an APS	Clause/ Subclause	Test defined in Clause/subclause
Additional requirements	7.3	E.5.1.1, E.5.1..2, E.5.1.3 E.5.1.4.1, E.6.1
Power available from an APS	7.3.1	E.5.1.4.1
APS switch-on time	7.3.2	E.6.1.1
APS switch-off time	7.3.3	E.6.1.2
APS power consumption when off	7.3.4	N/R
Dynamic behaviour of APS	7.3.5	N/R
Additional requirements for NT1 restricted mode source for compatibility with an APS	7.4	E.6.2
PS1 restricted mode back-off	7.4.1	E.6.2.1
PS1 restricted mode power up	7.4.2	E.6.2.2
NT1 power consumption from APS normal mode	7.4.3	E.6.2.3

E.1.4.10 Interface connector and contact assignments

Requirements	Clause/ Subclause	Test defined in Clause/subclause
Reference configuration of leads	A.9.1.1	E.2.1.1, E.5.1.1, E.5.1.2
Contact assignments	A.10	E.2.1.1, E.5.1.1, E.5.1.2

E.1.4.11 Annexes

Requirements	Clause/ Subclause	Test defined in Clause/subclause
Test loopbacks defined for the basic user-network interface	Annex A App. I	N/R
Additional requirements applicable to the explicit S reference point	Annex B	N/R
TE design to minimise power disturbance	Annex C	N/R

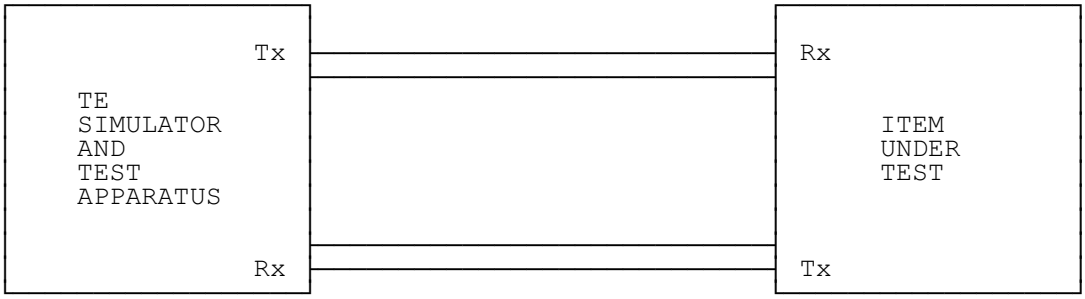
E.2 Functional characteristic tests (Clause A.5, ETS 300 012)

E.2.1 Binary organisation of frame (subclause A.5.4.2.2, ETS 300 012)

E.2.1.1 Test A

Purpose: To check the binary organisation of INFO 4 frames.

Test configuration:



System state: Active *(state G3)*, with pseudo-random pattern *(word length* $\geq 2^9$*-1)* in both B-channels and messages in the D-channel.

Stimulus: INFO 3 type frames from the TE simulator.

Monitor: The frame structure from the NT *(positive pulses, negative pulses and bit and frame timing are available).*

Results :

BIT POSITION	DESCRIPTION	POLARITY
1	F-bit	positive pulse
2	L-bit	negative pulse
3-10	B1 octet	first binary ZERO coded negative, the following bits may be positive, negative or no pulse
11	E-bit	logically equal to bit 47 of the previous frame in the TE-NT direction
12	D-bit	positive, negative or no pulse
13	A-bit	no pulse
14	Fa	negative, positive or in case of multiframing NT2 no pulse
15	N	opposite binary value of Fa
16-23	B2 octet	positive, negative or no pulse
24	E-bit	logically equal to bit 12 of the frame in the TE-NT direction
25	D-bit	positive, negative or no pulse
26	M	multiframing bit, negative, positive or in case of multiframing NT2 no pulse
27-34	B1 octet	positive, negative or no pulse
35	E-bit	logically equal to bit 25 of the frame in the TE-NT direction
36	D-bit	positive, negative or no pulse
37	S-bit	positive or negative pulse
38-45	B2 octet	positive, negative or no pulse
46	E-bit	logically equal to bit 36 of the frame in the TE-NT direction
47	D-bit	positive, negative or no pulse
48	L-bit	positive or no pulse

NOTE 1: L = balance bit which is used to ensure even parity of pulses in one frame.

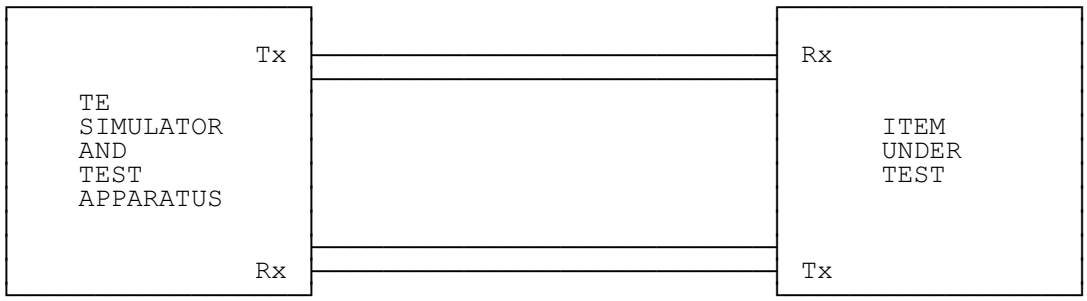
NOTE 2: See figure 3/I.430 [2] for details of pulse polarity.

NOTE 3: Multiframing procedure is not covered by this test.

E.2.1.2 Test B

Purpose: To check the binary organisation of INFO 2 frames.

Test configuration:



System state: Pending activation *(state G2)*.

Stimulus: Activation Request from the TE *(INFO 1)*.

Monitor: Line signals.

Results: Check that the B, D, D-echo channels, bits A, M and S are set to binary ZERO. Bits N and L are set according to the normal coding rules *(N and L set to binary ONE)*.

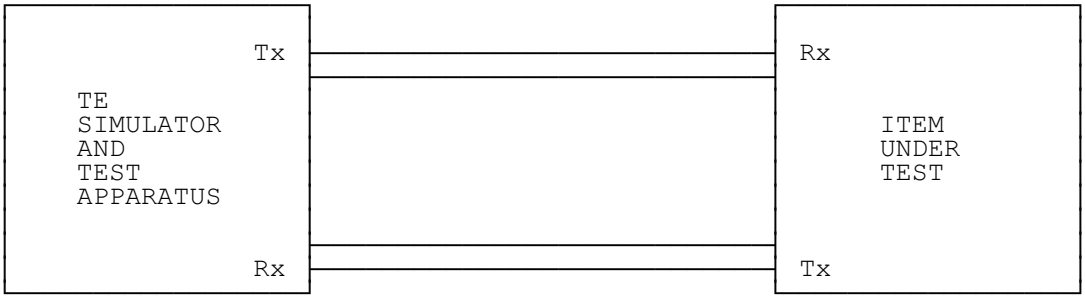
E.3 Interface procedure tests (Clause A.6, ETS 300 012)

These tests are designed to test conformance to the specification of the interface procedures. The tests are performed by stimulating and monitoring the interface I_b of an IUT from the I.430 [2] bus and by Activation Requests from the network or the terminal.

E.3.1 D-channel Interframe Time Fill (subclause A.6.1.1, ETS 300 012)

Purpose: To check the D-channel contains the correct Interframe Time Fill from the NT.

Test configuration:



System state: Active *(state G3)*.

Stimulus: INFO 3 from the TE simulator with binary ONE in the D-channel.

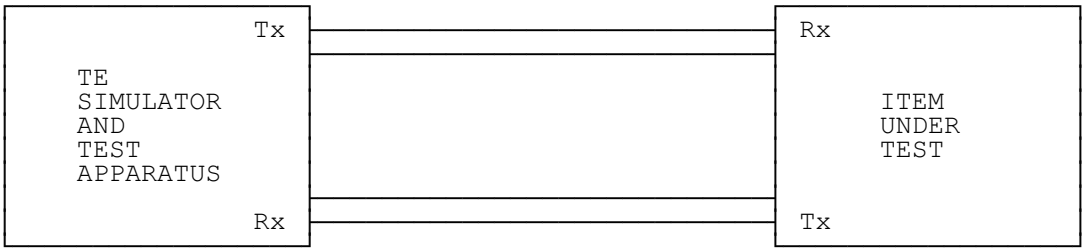
Monitor: D-channel.

Results: Binary ONEs or repetitions of "01111110".

E.3.2 D-echo channel response (subclause A.6.1.2, ETS 300 012)

Purpose: To check that the NT, on receipt of a D-channel bit from the TE simulator, reflects the binary value in the next available D-echo channel bit position towards the TE.

Test configuration:



System state: Active *(state G3)*.

Stimulus: INFO 3 from the TE simulator with binary ONEs and ZEROs in the D-channel.

Monitor: Receive D-channel from the TE and transmit D-echo channel by the NT.

Results: When the TE simulator sends a D-bit binary ZERO, the returned binary value in the next available D-echo channel bit position towards the TE shall be ZERO.

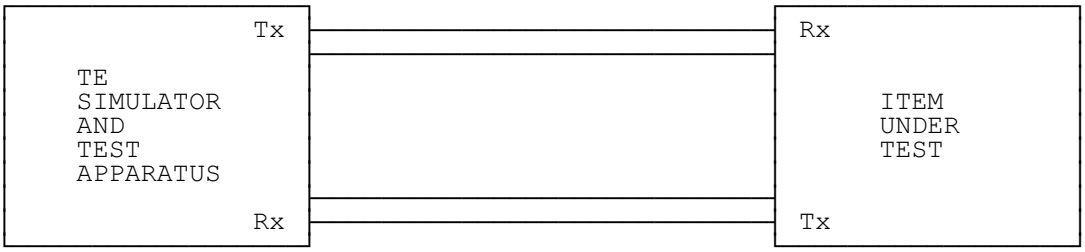
When the TE simulator sends a D-bit binary ONE, the returned binary value in the next available D-echo channel bit position towards the TE shall be ONE.

E.3.3 Activation/deactivation (subclause A.6.2, ETS 300 012)

E.3.3.1 Activation/Deactivation Procedure (subclause A.6.2, ETS 300 012)

Purpose: To check that the NT correctly executes the activation/deactivation procedure.

Test configuration:



System state: Any state.

Stimulus: Line signals INFOs 0, 1 and 3 applied from the TE simulator and Activation Request *(PH-AR)* applied from the network.

Monitor: Transmitted line signals, INFOs 0, 2 and 4.

Results : New state, transmitted signal (as described in the table below) and primitives sent to the higher layers according to table 6/I.430 [2].

STATE NO	CURRENT STATE	STIMULUS	NOTE	NEXT STATE	INFO SENT	COMMENT
1	G1	PH-AR	5	G2	I2	Initiate activation & T1
2	G1	T1 expires		G1	I0	No action
3	G1	T2 expires		G1	I0	No action
4	G1	Rx INFO 0	4	G1	I0	No action
5	G1	Rx INFO 1	5	G2	I2	Activation by the TE & T1
6	G2	MPH-DR	2	G4	I0	Initiate deactivation & T2
7	G2	T1 expires	2/5	G4	I0	Initiate deactivation & T2
8	G2	T2 expires		G2	I2	No action
9	G2	Rx INFO 0	4	G2	I2	No action
10	G2	Rx INFO 1		G2	I2	No action
11	G2	Rx INFO 3	3	G3	I4	Activate & stop T1
12	G3	MPH-DR	2	G4	I0	Initiate deactivation & T2
13	G3	T2 expires		G3	I4	No action
14	G3	Rx INFO 0	1/4	G2	I2	Pending deactivation
15	G3	Rx INFO 3		G3	I4	No action
16	G3	Lost framing		G2	I2	Loss of framing signalling
17	G4	PH-AR	5	G2	I2	Initiate activation & T1
18	G4	T1 expires		G4	I0	No action
19	G4	T2 expires	2	G1	I0	Deactivated
20	G4	Rx INFO 0	4	G1	I0	Deactivated
21	G4	Rx INFO 1		G4	I0	No action
22	G4	Rx INFO 3		G4	I0	No action
23	G4	Lost framing		G4	I0	No action

NOTE 1: For testing purposes INFO 0 is simulated by a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1 MHz).

The NT shall react by transmitting INFO 2 within a period time 250 µs to 25 ms.

NOTE 2: In case the value of timer T2 is 0, a direct transition from state G2 or G3 to G1 is possible (NOTE 2 of subclause A.6.2.6.2, ETS 300 012).

NOTE 3: A minimum period of 100 ms can elapse before the sending of INFO 4 or sending of the primitives PH-AI and MPH-AI (NOTE 4 of subclause A.6.2.6.2, ETS 300 012).

NOTE 4: INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received.

NOTE 5: Timer 1 is a supervisory timer which has to take the overall time to activate into account. This time includes the time it takes to activate both the ET-NT and the NT-TE sections of the customer access. ET is the exchange termination.

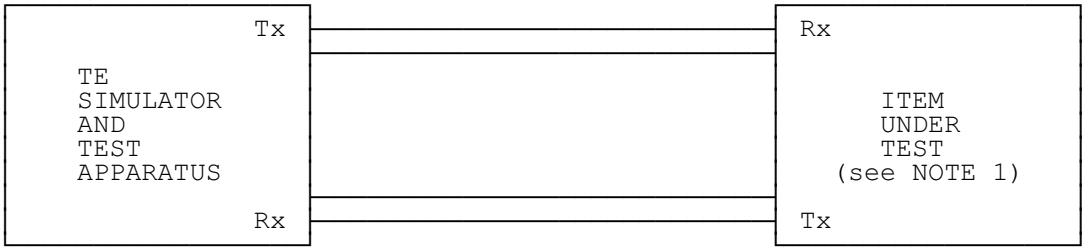
E.3.3.2 Activation/deactivation time (subclause A.6.2, ETS 300 012)

E.3.3.2.1 NT activation time (subclause A.6.2.6.2, ETS 300 012)

• Test A

Purpose: To check the value of the NT activation time.

Test configuration:



NOTE 1: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Deactive state *(state G1)*.

Stimulus: INFO 1 from the TE simulator continuously.

Monitor: The line signals measuring the elapsed time between start of receipt of INFO 1 and transmission of INFO 2.

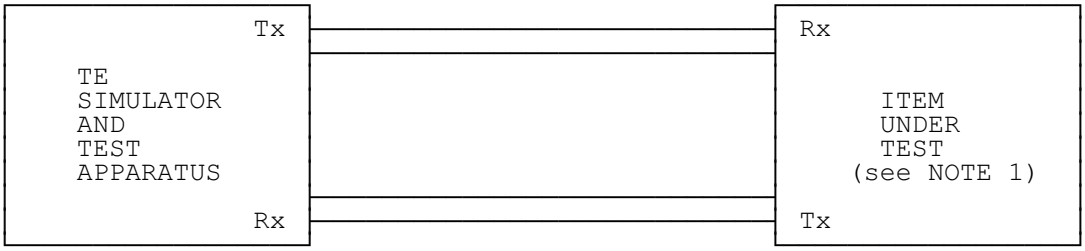
Results: INFO 2 should be started within 1 s upon the receipt of the first INFO 1.

NOTE 2: Delays "Da" as long as 30 s are acceptable under abnormal conditions *(no fault)*.

• Test B

Purpose: To check the value of the NT activation time.

Test configuration:



NOTE 1: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Pending activation *(state G2)*.

Stimulus: INFO 3 from the TE simulator.

Monitor: The line signals measuring the elapsed time between start of receipt of INFO 3 and transmission of INFO 4.

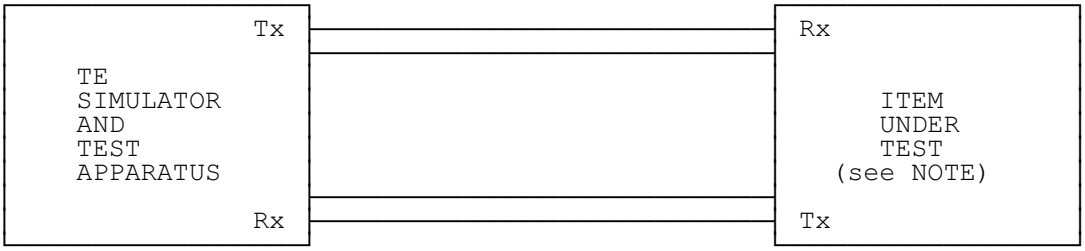
Results: INFO 4 should be started within 1 s upon the receipt of INFO 3.

Delays "Db" as long as 15 s are acceptable under abnormal conditions *(no fault)*. The sum of delays "Da" and "Db" shall be ≤ 30 s. *(see NOTE 2 of subclause E.3.3.2.1)*.

E.3.3.2.2 Deactivation time (subclause A.6.2.7, ETS 300 012)

Purpose: That a NT responds to the receipt of INFO 0 by initiating the transmission of INFO 2 within a period of 250 µs to 25 ms.

Test configuration:



NOTE: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Active *(state G3)*.

Stimulus: INFO 0 from the TE simulator *(see NOTE 1 in subclause E.3.3.1).*

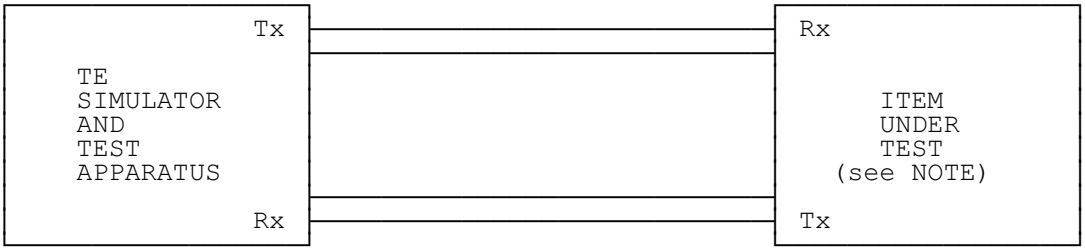
Monitor: The line signals measuring the elapsed time between :
Receiving INFO 0 *(cessation of INFO 3)* from the TE and sending INFO 2 from the NT.

Results: INFO 4 ceases *(INFO 2 begins)* within 250 µs and 25 ms.

E.3.3.2.3 Value of the timer T2 (subclause A.6.2.6.2, ETS 300 012)

Purpose: To check the value of Timer T2.

Test configuration:



NOTE: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Pending activation *(state G2)*.

Stimulus: Expiration of Timer T1.
INFO 1 from the TE simulator.

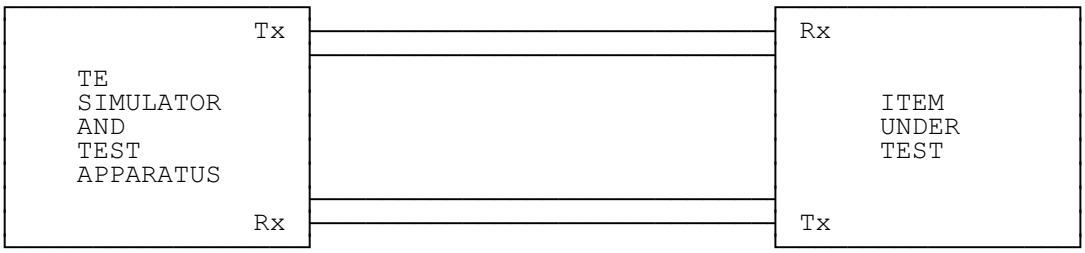
Monitor: The line signals measuring the elapsed time between the cessation of INFO 2 and sending another time INFO 2.

Result: 25 ms ≤ T2 ≤ 100 ms.

E.3.4 Frame alignment procedures (subclause A.6.3, ETS 300 012)

Purpose: To test that the NT correctly executes the frame alignment procedures *(enter frame alignment)*.

Test configuration:



System state: Active *(state G3)*.

Stimulus: Good/bad frames from the TE simulator.

NOTE 1: A bad frame is simulated by any bit pattern with violation of the coding rules on which the IUT conforming to subclause A.6.3.1.2 of ETS 300 012 is not able to detect the frame alignment.

NOTE 2: The start of a frame is defined to the position where the F-bit according to figure 3/I.430 [2] should appear.

Monitor: Received and transmitted line signals.

Results:

	STIMULUS	**RESULTS**	**COMMENTS**
a)	1 bad frame *(see 1))*	INFO 4	No loss of framing
b)	n bad frames *see 1) and 4))*	INFO 2	Framing lost
c)	m good frames *(see 2), 3) and 5))*	INFO 4	Framing regained within 4 frames

1) Before the commencement of the test, the NT shall be in system state G3.

2) Before the test the NT shall **not** be in system state G3.

3) Multiframing procedure is not covered by this test.

4) The value of n *($n \geq 2$)* shall be provided by the supplier of the IUT before the test.

5) The value of m *(corresponding to at least 3 consecutive pairs of line code violations)* shall be provided by the supplier of the IUT before the test.

E.4 Electrical characteristic tests (Clause A.8, ETS 300 012)

These tests are designed to check that the interface conforms to the electrical characteristics specified in Clause A.8, ETS 300 012.

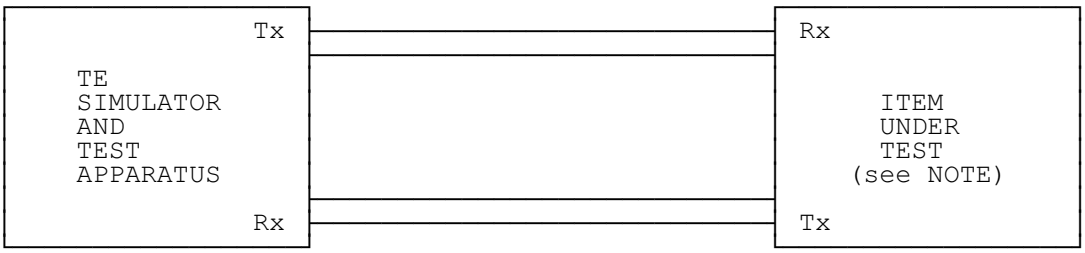
Many of these tests require the interface to be stable in the activated state and transmitting a specific bit pattern, with or without the connection to the TE. As none of these requirements can be met with the TE simulator operating normally, it is anticipated that special arrangements shall be made to permit this, for example the receiving section of the TE Simulator could be set in the appropriate state manually.

E.4.1 Bit rate (subclause A.8.1, ETS 300 012)

E.4.1.1 Bit rate when transmitting an INFO 2 (subclause A.8.1.1 and A.8.1.2, ETS 300 012)

Purpose: The average bit rate when the NT is transmitting INFO 2 type frame.

Test configuration:



NOTE: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Pending activation *(state G2)*.

Stimulus: INFO 1 type frames from the TE simulator.

Monitor: Bit rate.

Results: a) Basic rate access element:

nominal bit rate of 192 kHz (related to the network clock accuracy is given in CCITT Recommendations Q.512 [15] and G.812 [16] as far as the I_b point is concerned).

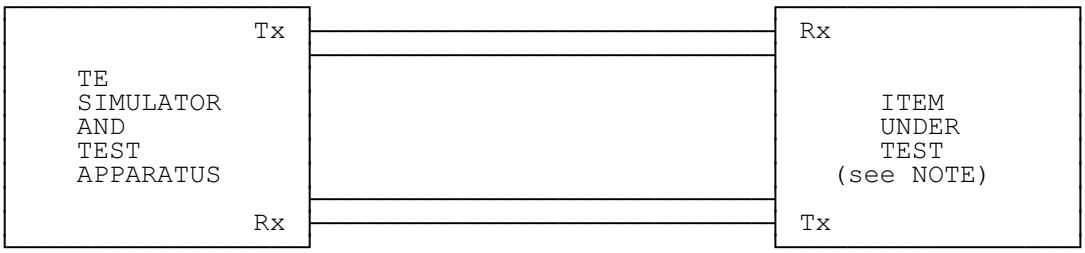
b) NT2 in free running mode:

bit rate of 192 kHz ± 100 ppm.

E.4.1.2 Bit rate when transmitting an INFO 4 (subclause A.8.1.1 and A.8.1.2, ETS 300 012)

Purpose: The average bit rate when the NT is transmitting an INFO 4 type frame.

Test configuration:



NOTE: If the item under test is not a NT2, the test configuration shall also include the subscriber line, the access network and the exchange termination.

System state: Active *(state G3)*.

Stimulus: INFO 3 type frames from the TE simulator.

Monitor: Bit rate.

Results:

a) Basic rate access element:

nominal bit rate of 192 kHz (related to the network clock accuracy is given in CCITT Recommendations Q.512 [15] and G.812 [16] as far as the I_b point is concerned).

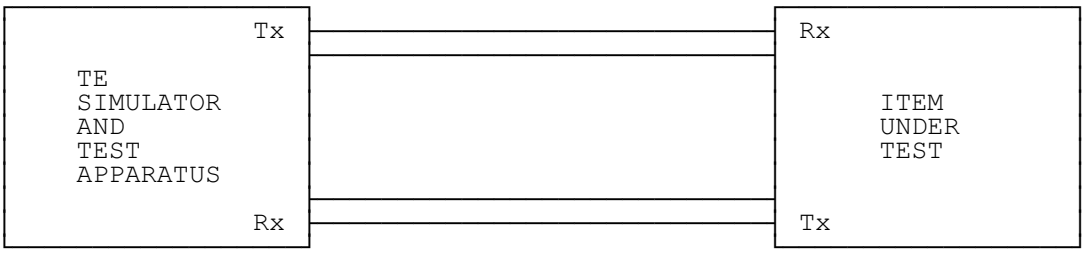
b) NT2 in free running mode:

bit rate of 192 kHz ± 100 ppm.

E.4.2 NT jitter characteristics (subclause A.8.3, ETS 300 012)

Purpose: NT output jitter when transmitting INFO 4.

Test configuration:



System state: Active *(state G3)*.

When IUT sending :
a) binary ONEs in D and both B-channels,
b) a sequence consisting of a pseudo random pattern with a length of 2^{19}-1 in D and both B-channels *(see NOTE)*.

Stimulus: INFO 3 type frames from the TE simulator with pseudo-random pattern with a length of 2^{19}-1 in D-channel and with the stimulating signal to the interface from which the timing will be derived containing the maximum tolerable jitter at the synchronising input of the IUT.

Monitor: The jitter should be measured using a high pass filter having a cut-off frequency *(3 dB point)* of 50 Hz and an asymptotic roll-off of 20 dB per decade.

Results: The maximum jitter *(peak to peak)* shall be less than 5 % of a bit period.

NOTE: For testing purpose of NT2, a fixed pattern in D-channel can be acceptable *(binary ONE or flags)*.

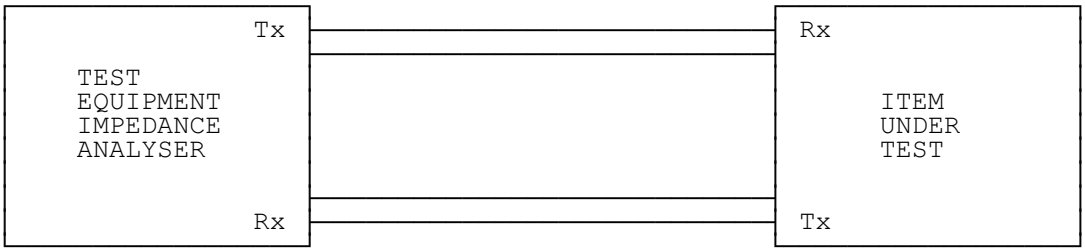
E.4.3 NT transmitter output impedance (subclause A.8.5.1.1, ETS 300 012)

NOTE: NT transmitting pair connected without its terminating resistor.

E.4.3.1 Test A

Purpose: Output impedance of the transmitter when transmitting a binary ONE *(no signal)*.

Test configuration:



If the IUT provides PS1 normal, the condition a) shall be used, otherwise condition b).

a) using configuration with maximum power *(at least 1 W)* from Power Source 1 in normal power condition.

b) using configuration with maximum power *(420 mW)* drawn from Power Source 1 in restricted power condition.

System state: Deactive *(state G1)*.

Stimulus: Sinusoidal voltage of 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

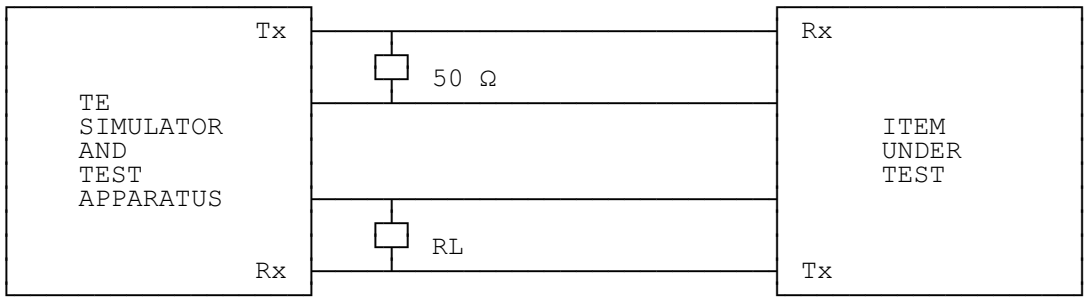
Monitor: Impedance.

Results: The measured value shall exceed the impedance template of figure 11 of I.430 [2].

E.4.3.2 Test B

Purpose: Output impedance of the transmitter when transmitting a binary ZERO.

Test configuration:



If the IUT provides PS1 normal, the condition a) shall be used, otherwise condition b).

a) using configuration with maximum power *(at least 1 W)* from Power Source 1 in normal power condition.

b) using configuration with maximum power *(420 mW)* drawn from Power Source 1 in restricted power condition.

System state: Active *(state G3)*.

Stimulus: INFO 3.

Monitor: Both positive and negative pulses.

The output impedance limit shall apply for a nominal load impedance *(resistive)* condition : RL = 50 Ω. The output impedance for this nominal load is defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10 %.

The peak amplitude is defined as the amplitude of the midpoint of the pulse. The test applies for pulses of both polarities.

Results: The output impedance shall be R ≥ 20 ohms.

$$R = \frac{U_+ - U_-}{U_-/R_- - U_+/R_+}$$

R_+ : nominal resistance R_L + 10 %.
R_- : nominal resistance R_L - 10 %.

U_+ : peak amplitude when R_+ is applied.
U_- : peak amplitude when R_- is applied.

E.4.4 Pulse shape and amplitude (subclause A.8.5.3, ETS 300 012)

Purpose: Pulse shape and amplitude of isolated transmitted pulses.

Test configuration: IUT interface transmitting pair terminated in 50 ohms.

System state: Active *(state G3)*.

Stimulus: INFO 3.

Monitor: Both positive and negative isolated pulses.

Results: Both positive and negative pulses shall be within the mask of figure 13 of I.430 [2] with a nominal amplitude of 750 mV, zero to peak *(see also subclause A.8.5.3.1, ETS 300 012)*.

E.4.5 Pulse unbalance (subclause A.8.5.4, ETS 300 012)

E.4.5.1 Pulse amplitude (subclause A.8.5.4.1, ETS 300 012)

Purpose: Pulse amplitude when transmitting a high density pattern.

Test configuration: IUT interface transmitting a pair terminated in 50 Ω.

System state: Pending activation *(state G2)*.

Stimulus: INFO 1.

Monitor: The amplitude of positive and negative pulses at the midpoint of the pulse.

Results: The measured amplitude in the midpoint of the pulse shall be within the ± 10 % of the nominal amplitude values. The measurement must be done on 40 continuous frames.

E.4.5.2 Pulse unbalance of an isolated couple of pulses (subclause A.8.5.4.2, ETS 300 012)

Purpose: The relative difference in integral Udt for positive and negative pulses.

Test configuration: IUT interface transmitting pair terminated in 50 Ω.

System state: Active *(state G3).*
IUT transmitting INFO 4 *(see NOTE).*

NOTE: for NTs conformance test shall be done with the signal INFO 4. In the B1-channel two alternated octets 1111 1111 and 1111 1100 shall be inserted so that the two binary ZEROs are set in the bit position 33 and 34 *(see table 3/I.430 [2])*. All B2-, D- and E-bits shall be set to binary ONE.

Stimulus: INFO 3.

Monitor: a) voltage when transmitting INFO 0,
b) isolated couple of pulses.

Results: The absolute sum *(NOTE)* of the integral Udt for a positive pulse and the integral Udt for a negative pulse shall be less than, or equal to, 5 % of the nominal pulse. The zero reference voltage is given by the signal when transmitting INFO 0.

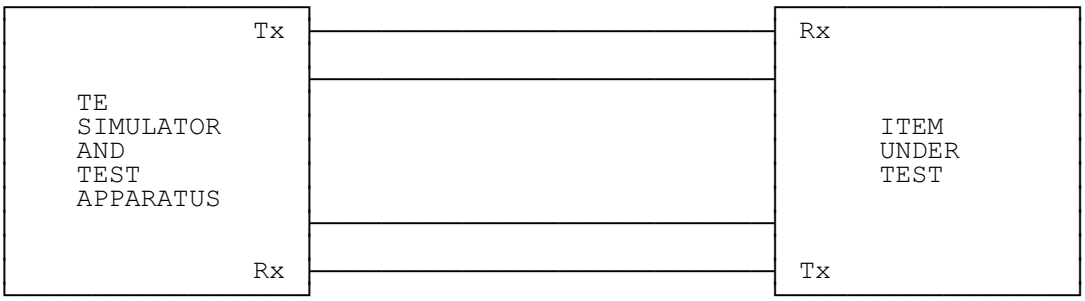
NOTE: The edge between the two adjacent pulses is the crossing of the zero voltage. From this edge, the integral is defined for a time period of 1,5 UI in each direction.

E.4.6 Longitudinal conversion loss of transmitter output (subclause A.8.5.6.1, ETS 300 012)

NOTE: NT transmitter pair connected without terminating resistors.

Purpose: Longitudinal Conversion Loss (LCL) (the ratio of longitudinal signal converted to a transverse signal as a result of the unbalance about earth of the output of the Item Under Test).

Test configuration:



System state: Deactive *(state G1)*.

Stimulus: 1 volt rms longitudinal in accordance with figure 15/I.430 [2].

Monitor: Transverse voltage in accordance with figure 15/I.430 [2] with selective level measuring instrument.

Results:

FREQUENCY	LONGITUDINAL CONVERSION LOSS
10 kHz ≤ f ≤ 300 kHz 300 kHz ≤ f ≤ 1 MHz	≥ 54 dB Minimum value decreasing from 54 dB at 20 dB/decade.

E.4.7 Receiver input characteristics (subclause A.8.6, ETS 300 012)

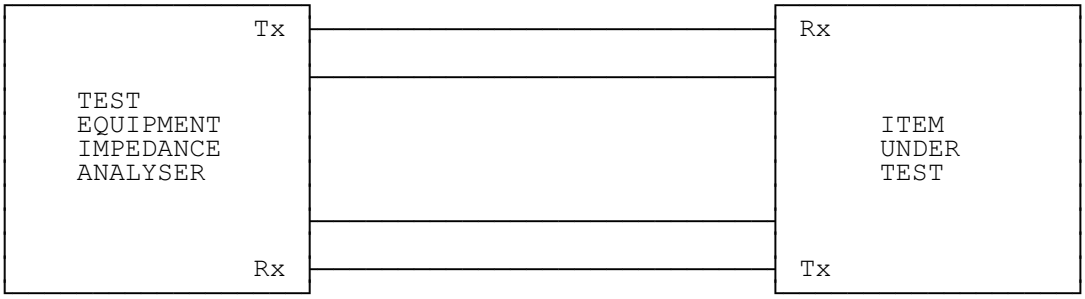
E.4.7.1 NT receiver input impedance (subclause A.8.6.1.2, ETS 300 012)

NOTE: NT receiving pair connected without its terminating resistor.

E.4.7.1.1 Test A

Purpose: To test the input impedance of a NT whilst in a deactive state.

Test configuration:



If the IUT provides PS1 normal, the condition a) shall be used, otherwise condition b).

a) using configuration with maximum power *(at least 1 W)* from Power Source 1 in normal power condition.

b) using configuration with maximum power *(420 mW)* drawn from Power Source 1 in restricted power condition.

System state: Deactivated *(state G1)*.

Stimulus: Sinusoidal voltage of 100 mV rms, in the frequency range 2 kHz to 1000 kHz.

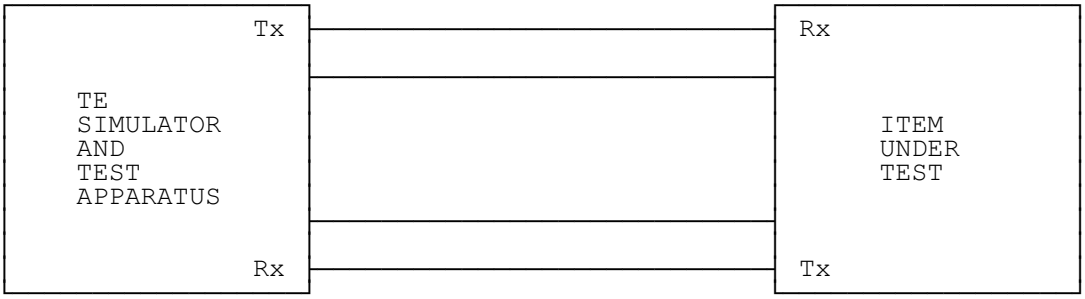
Monitor: Impedance.

Results: Shall exceed the impedance template of figure 11/I.430 [2].

E.4.7.1.2 Test B

Purpose: To test that the input impedance of the receiver is correct when receiving an overvoltage signal.

Test configuration:



If the IUT provides PS1 normal, the condition a) shall be used, otherwise condition b).

a) using configuration with maximum power *(at least 1 W)* from Power Source 1 in normal power condition.

b) using configuration with maximum power *(420 mW)* drawn from Power Source 1 in restricted power condition.

System state: Deactivated *(state G1)*.

Stimulus: Sinusoidal voltage of 1,2 V, zero to peak, applied at a frequency of 96 kHz *(the applied voltage to be monitored to ensure peak values are correct)*.

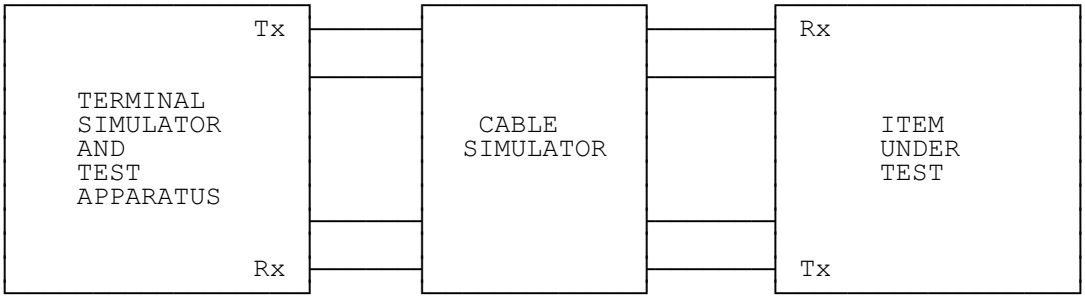
Monitor: Input current.

Results: The peak current shall not exceed 0,5 mA peak value.

E.4.7.2 Receiver sensitivity - Noise and distortion immunity (subclause A.8.6.2, ETS 300 012)

Purpose: Subclause A.8.6.2 of ETS 300 012 is designed to correctly test the receiver's function in the various wiring configurations.

Test configuration:



System state: Active *(state G3)*.

Stimulus: Input signals are transmitted from the terminal simulator with a pseudo-random sequence *(word length ≥ 511 bits)* in both B-channels with amplitudes, delay and interfering signals as detailed in subclause A.8.6.2.2 to subclause A.8.6.2.5, ETS 300 012.

When performing this test the error rate measurement can be made either after the receiver using a B-channel access port or at the IUT transmitter. If the measurement is at the NT transmitter, then the connection to the TE simulator should be made through a time delay corresponding to the bus configuration used.

The following amplitudes are provided by the TE simulator corresponding to the bus configuration as given in subclause A.8.2.1, ETS 300 012.

Monitor:

Condition on NT	Clause/ subclause	Configuration	Amplitude relative to the nominal one
For short passive bus	A.8.6.2.2	ii and iii	- 1.5 dB and + 1.5 dB at the TE output
For point-to-point and short passive bus (see NOTES 1 and 2)	A.8.6.2.3	i ii iii iv	- 1.5 dB at the TE simulator output - 1.5 dB and + 1.5 dB at the TE output - 1.5 dB and + 1.5 dB at the TE output + 1.5 dB at the TE simulator output
For extended bus (see NOTE 2)	A.8.6.2.4	iv see NOTE 3	+ 1.5 dB at the TE simulator output - 1.5 dB at the TE simulator output
For point-to-point (see NOTES 1 and 2)	A.8.6.2.5	i iv	- 1.5 dB at the TE simulator output + 1.5 dB at the TE simulator output

NOTE 1: In addition jitter-up to the maximum permitted (subclause A.8.2.2, ETS 300 012) in the output signal of TE is superimposed on the input signals.

NOTE 2: Additionally the IUT shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals.

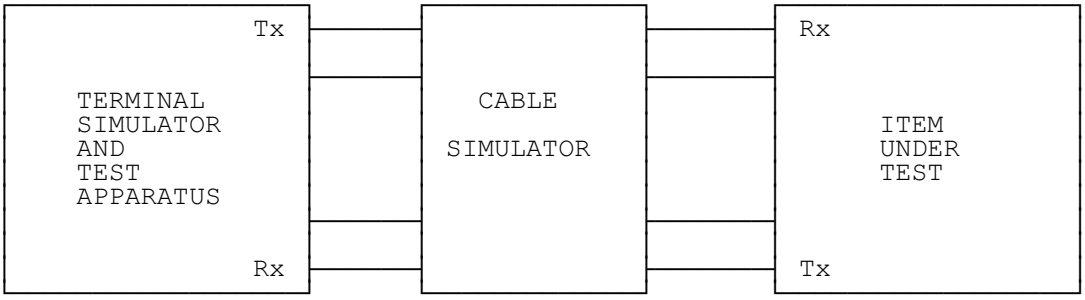
NOTE 3: This configuration consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120 nF/km, a loss of 3,8 dB at 96 kHz, four TEs connected such that the differential delay is at the maximum permitted by subclause A.8.6.3.3, ETS 300 012.

Results: No error for a monitoring period of at least one minute.

E.4.7.3 NT receiver input delay characteristics (subclause A.8.6.3, ETS 300 012)

Purpose: Test of error free transmission with permitted round trip delay.

Test configuration:



System state: Pending activation (state G2).

Condition on NT	Clause/ subclause	Configuration	Round trip delay
For short passive bus	A.8.6.3.1	ii and iii	10 to 14 µs
For point-to-point and passive bus	A.8.6.3.2	i ii and iii	10 to 42 µs 10 to 13 µs
For extended bus	A.8.6.3.3	see NOTE	10 to 42 µs
For point-to-point	A.8.6.3.4	i	10 to 42 µs

NOTE: This configuration consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120 nF/km, a loss of 3.8 dB at 96 kHz, four TEs connected such that the differential delay of signals from different TEs is in the range 0 to 2 µs.

Stimulus: INFO 3 from the TE simulator.

A pseudo-random sequence (word length at least 511 bits) in both B-channels.

When performing this test the error rate measurement can be made either after the receiver using a B-channel access port or at the IUT transmitter. If the measurement is at the NT transmitter, then the connection to the TE simulator should be made through a time delay corresponding to the bus configuration used.

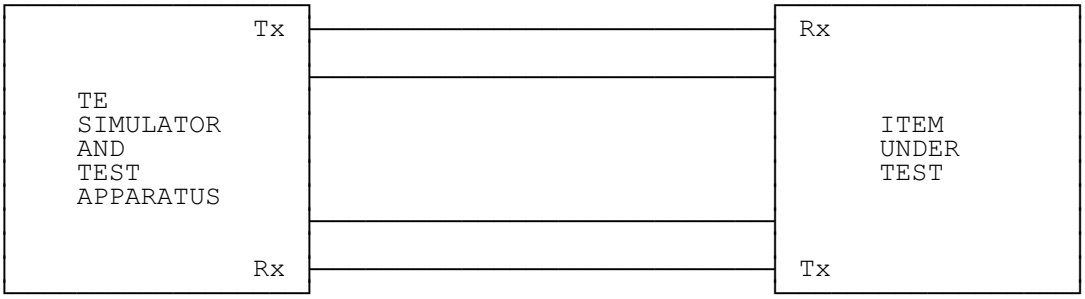
Monitor: Transmitting line signals from the IUT.

Results: IUT shall go to state G3. No error for a monitoring period of a least one minute.

E.4.7.4 Unbalance about earth of the receiver input (subclause A.8.6.4, ETS 300 012)

NOTE: NT receiver pair connected without terminating the resistors.

Purpose: Longitudinal Conversion Loss *(LCL) (the ratio of longitudinal signal converted to a transverse signal as a result of the unbalance about earth output of the Item Under Test)*.Test configuration:



System state: Deactive *(state G1)*, and active *(state G3)*.

Stimulus: 1 volt rms longitudinal in accordance with figure 15/I.430 [2].

Monitor: Transverse voltage in accordance with figure 15/I.430 [2] with selective level measuring instrument.

Results:

FREQUENCY	LONGITUDINAL CONVERSION LOSS
10 kHz ≤ f < 300 kHz 300 kHz ≤ f ≤ 1 MHz	≥ 54 dB Minimum value decreasing from 54 dB at 20 dB/decade.

E.5 Power feeding (Clause A.9, ETS 300 012)

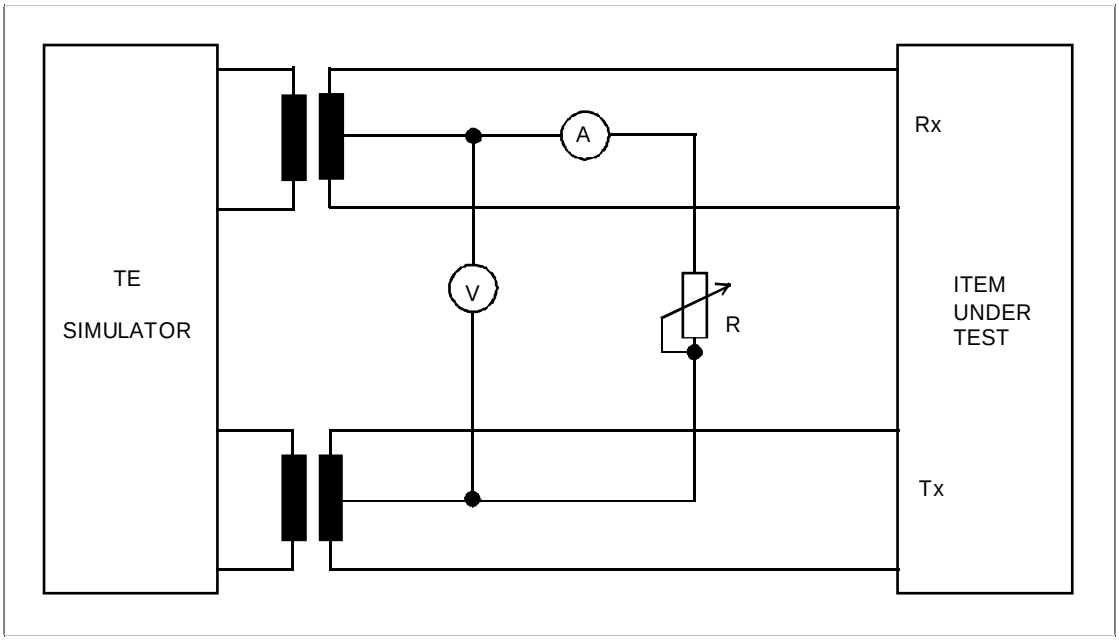
E.5.1 Power source 1

E.5.1.1 Normal power condition (subclause A.9.2.2.1, ETS 300 012)

NOTE: This requirement also applies to the APS.

Purpose: To ensure that the NT, whilst in Normal Power Condition, is feeding enough power to the S/T-bus from the Local Power Supply and to test the tolerance of the feeding voltage.

Test configuration:



System state: Any state.

Stimulus: Drawing no power and the maximum power provided by PS1 as declared by the apparatus supplier. Reduce the resistance from infinity ohms to a value, so that the maximum power is available.

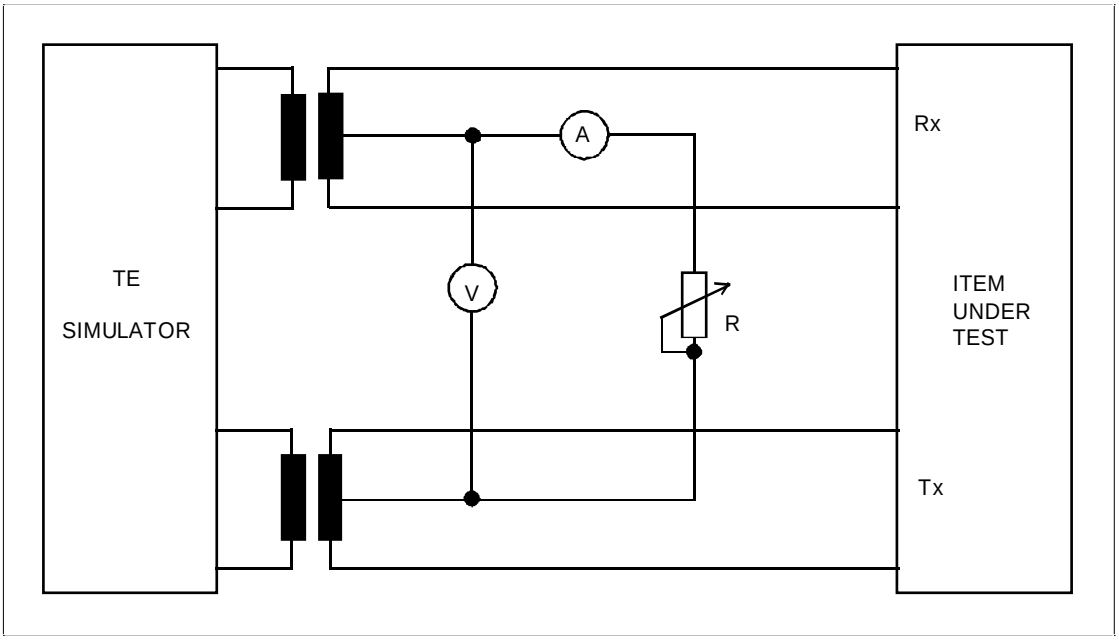
Monitor: DC voltage and current.

Results: The voltage at the output of the source shall be 40 V *(+ 5 / - 15 %)*.

E.5.1.2 Restricted power condition (subclause A.9.2.2.2, ETS 300 012)

Purpose: To ensure that the NT, under Restricted Power Condition, is feeding enough power to the S/T-bus from the line and to test the open circuit voltage.

Test configuration:



System state: Any state.

Stimulus: Drawing no power and the maximum power provided by PS1 as declared by the apparatus supplier. Reduce the resistance from infinity ohms to a value, so that the maximum power is available.

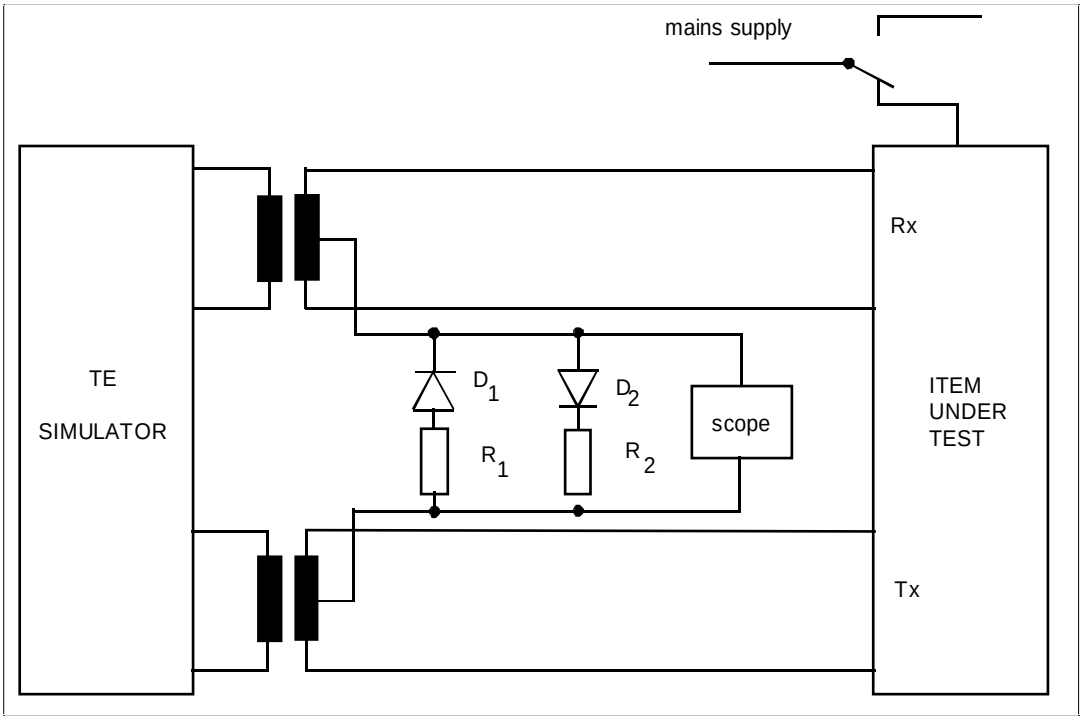
Monitor: DC voltage and current.

Results: The voltage at the output of the source shall be 40 V *(+ 5/ -15 %) (reversed polarity)*.

E.5.1.3 Power source switch-over time (subclause 7.1.2.1, ETS 300 012)

Purpose: To test switch-over time.

Test configuration:



The power consumption of D_1 and R_1 respesents a load of 420 mW (restricted mode). The power consumption of D_2 and R_2 represents a load of n*1W (normal mode).

System State: Any state.

Stimulus: Connection or disconnection of mains supply.

Monitor: Output-voltage versus time.

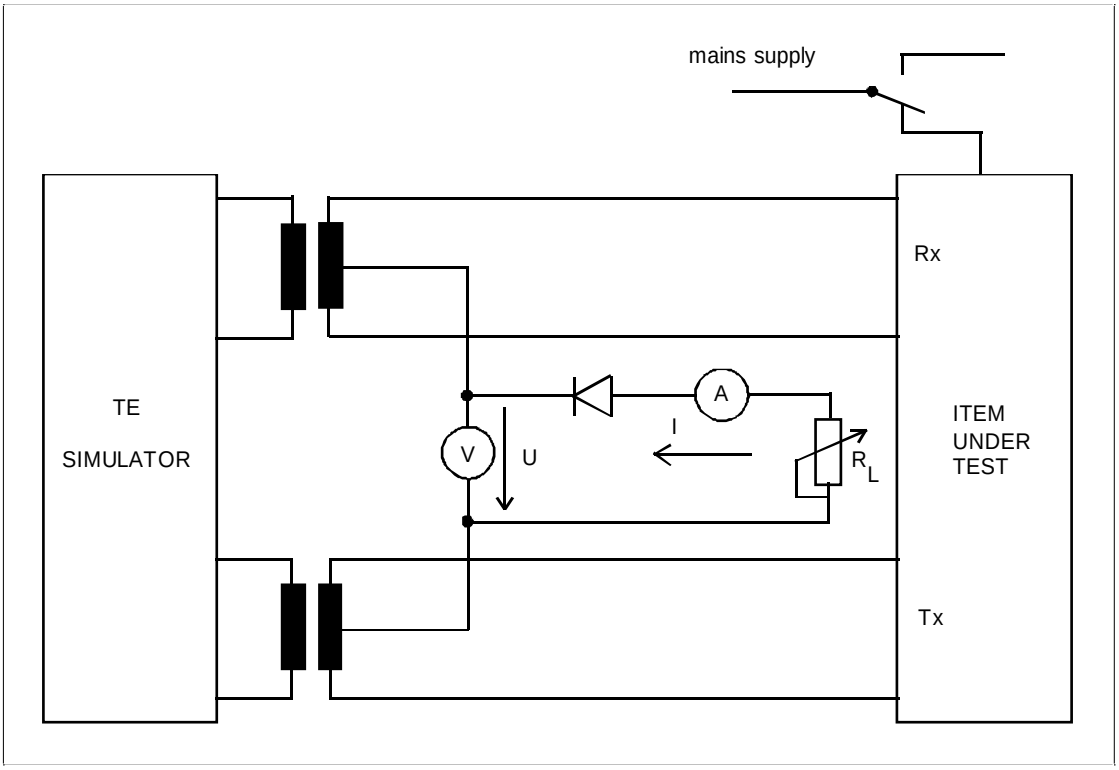
Results: The transition time of voltage between + 34 V and - 34 V *(or vice versa)* shall be less than 5 ms.

E.5.1.4 Power source 1 restricted mode under overload conditions (subclause 7.1.2.2, ETS 300 012)

E.5.1.4.1 Test A (subclause 7.1.2.2, ETS 300 012)

Purpose: Restricted mode power source requirements under overload conditions *(short-circuit current)*.

Test configuration:



System State: Any state.

Stimulus: Disconnection of mains supply and adjustment of the resistor R_L so that the voltage U is forced to a value ≤ 1 V.

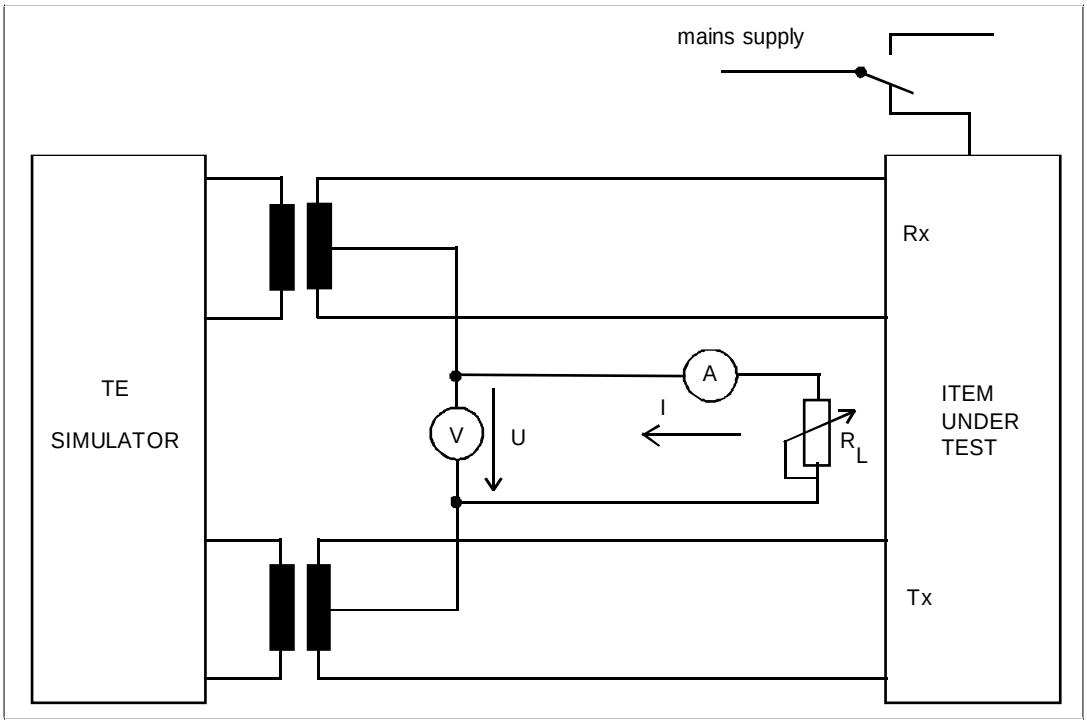
Monitor: Output-current.

Results: Minimal output current equal or greater than 9 mA at output voltage less than 1 V. This output current is measured for 1 second starting 1 second after the switch over is completed.

E.5.1.4.2 Test B (subclause 7.1.2.2, ETS 300 012)

Purpose: Restricted mode power source requirements under overload conditions *(load resistance increasing from short-circuit).*

Test configuration:



System State: Any state.

Stimulus: Increasing load resistor R_L starting with short-circuit.

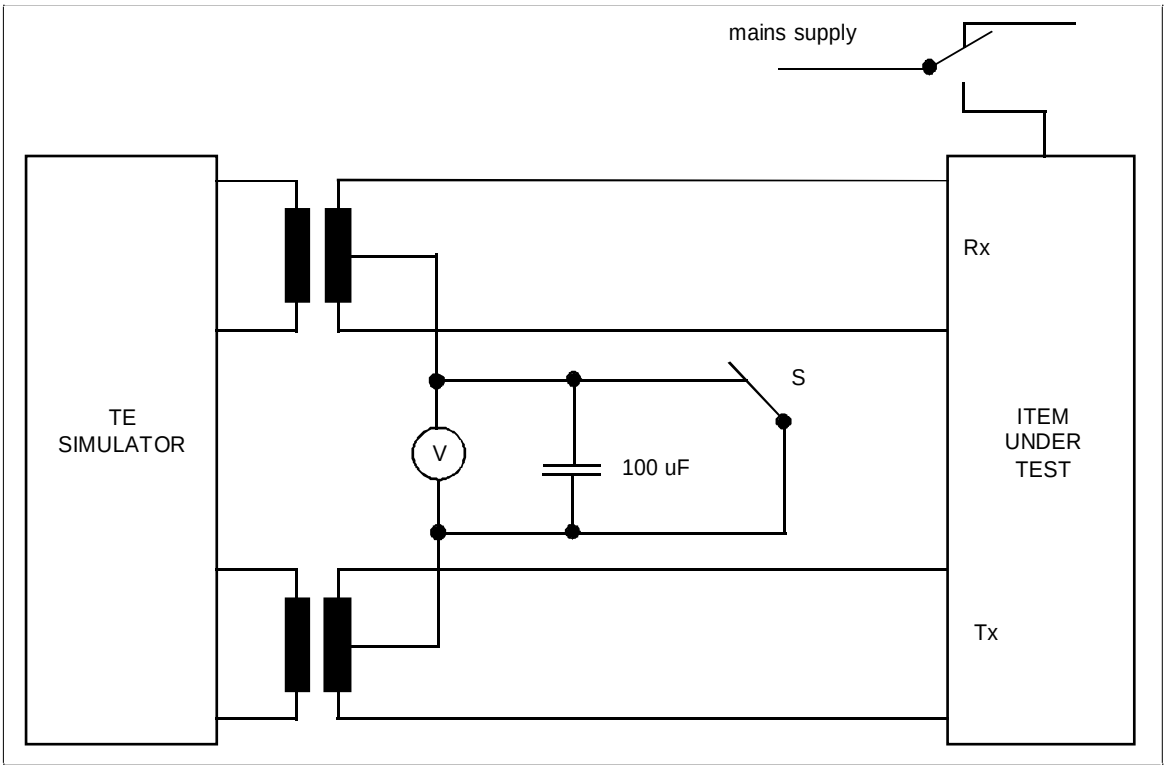
Monitor: Output current, output voltage.

Results: Output current shall be $I \geq 11$ mA at output voltage of U = 34 V.

E.5.1.4.3 Power source 1 restricted (Test C) (subclause 7.1.2.2, ETS 300 012)

Purpose: Restricted mode power source requirements under overload conditions *(load resistance decreasing from nominal output power).*

Test configuration:



System State: Any state.

Stimulus: Decreasing load resistor R_L, starting with load for nominal output power.

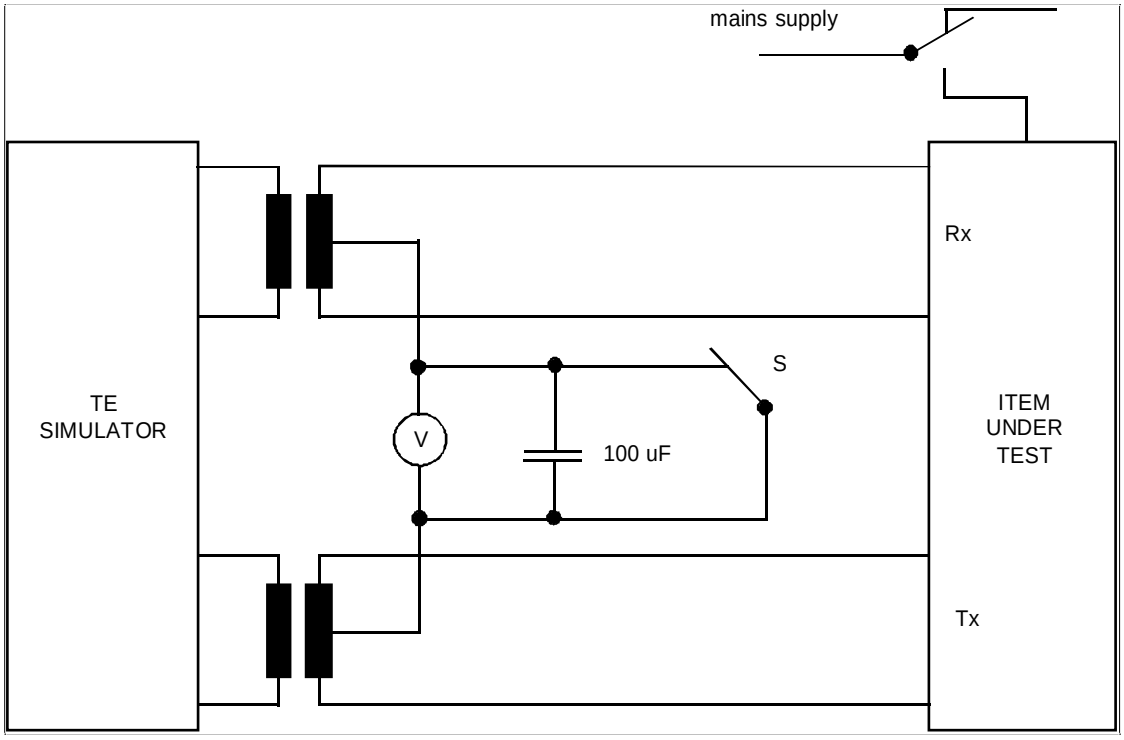
Monitor: Output current, output voltage.

Results: Output current shall be ≥ 11 mA at output voltage of 34 V.

E.5.1.4.4 Power source 1 restricted (Test D) (subclause 7.1.4.1, ETS 300 012)

Purpose: Capability to increase output voltage under capacitive load in restricted mode.

Test configuration:



System State: Any state.

Stimulus: Short-circuit for 30 minutes then removal of short-circuit *(switch off : S)*.

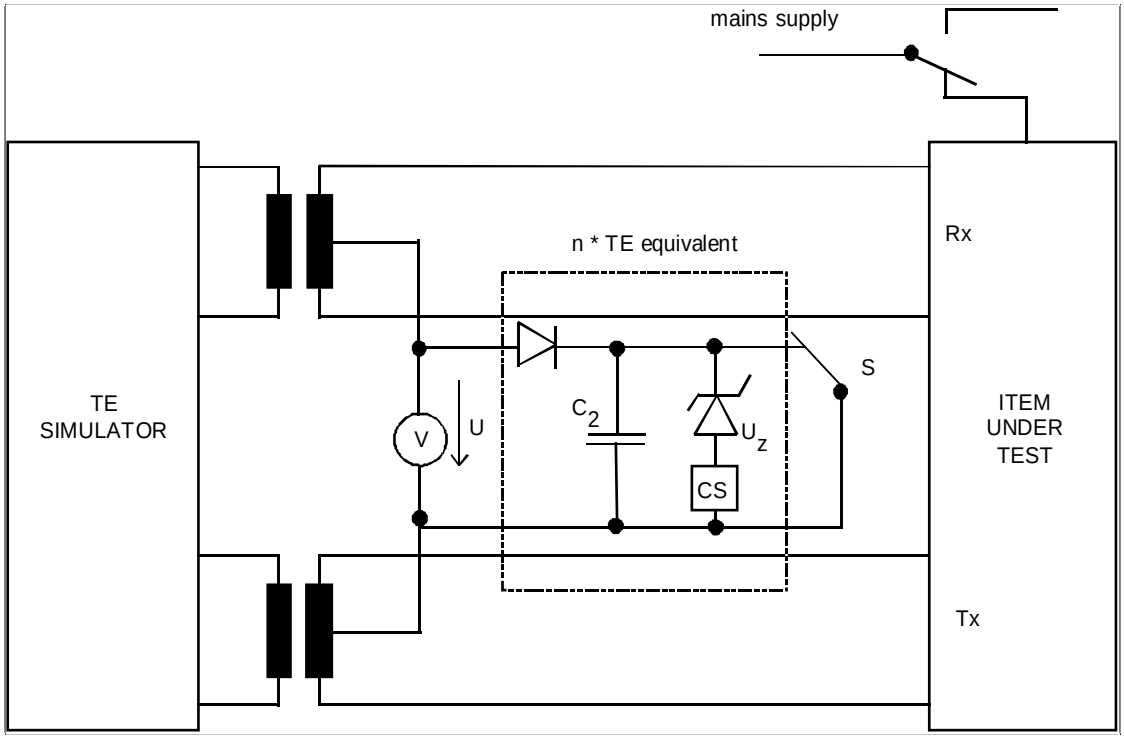
Monitor: Output voltage under capacitive load of 100 µF.

Results: Output voltage shall increase from 1,0 V to 34 V within 1,5 sec. This shall occur within 10 seconds after the removal of the short-circuit.

E.5.1.5 Requirements for type "a" sources (subclause 7.1.4.3, ETS 300 012)

Purpose: To test requirements for the voltage increase of a power source 1 normal, with fall-back characteristics, after removal of a short circuit.

Test configuration:



System State: Any state.

Stimulus: Lowest acceptable voltage level at mains interface, short-circuit steady state of 30 minutes, removal of short-circuit *(switch off : S)*, with a load of n TE-equivalents as given in figure 4/ ETS 300 012.

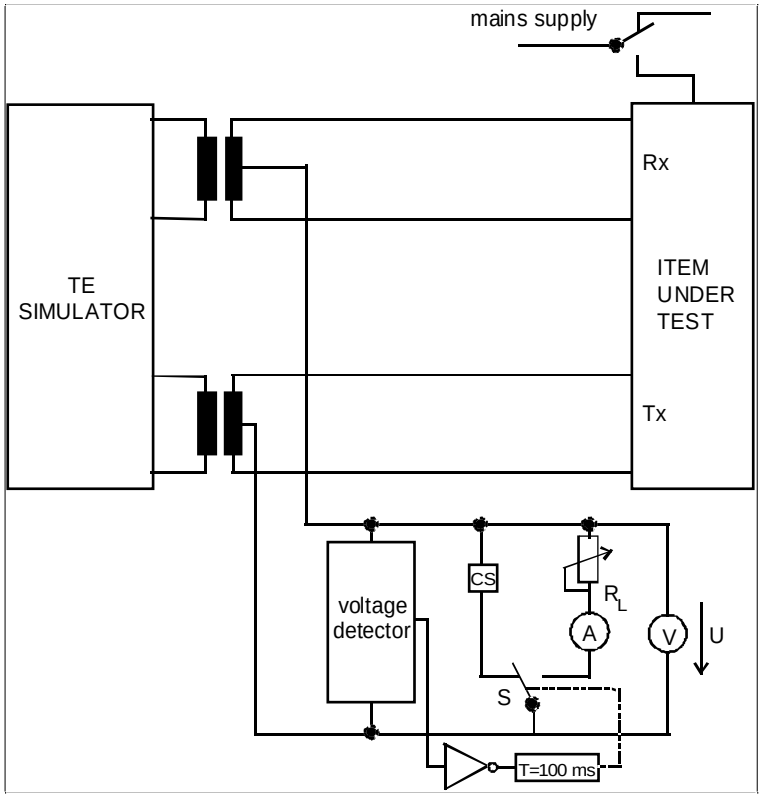
Monitor: Output voltage under n-times TE-equivalents.

Results: Output voltage shall increase from 1,0 V to 34 V within 350 msec. This shall occur within 10 seconds after the removal of the short circuit.

E.5.1.6 Switch on surge capability (subclause 7.1.4.4.1, ETS 300 012)

Purpose: Switch-on surge capability, power source 1 in normal mode.

Test configuration:



NOTE: If restricted power is provided prior to switch over to normal mode, protection of the current sink may be required.

System State: Any state.

Stimulus: Connection of mains supply.

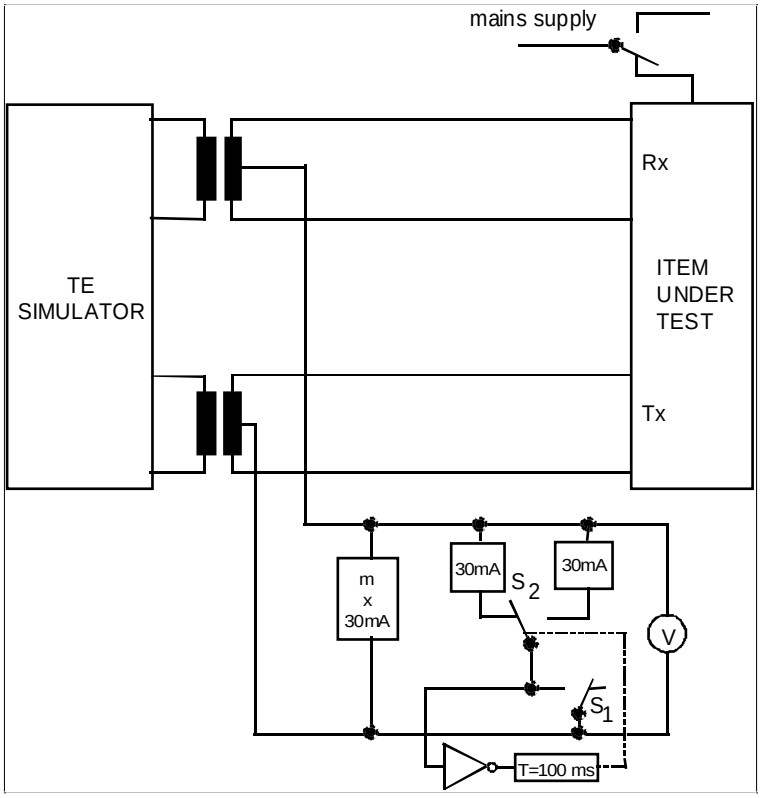
Monitor: Output voltage versus time.

Results: The power source 1 shall provide a minimum current of n times 45 mA (CS) for at least 100 ms and the voltage shall be at least 30 V during this time period. After the time of 100 ms, the power source shall be able to provide the power of n times 1 Watt (R_L) and the drop of power on the interface with the output voltage shall be within the specified limits.

E.5.1.7 TE connection surge capability (subclause 7.1.4.4.2, ETS 300 012)

Purpose: TE connection surge capability in normal mode.

Test configuration:



System State: Any state.

Stimulus: Switch on S_1 and then after a delay of 100 ms switch on S_2.

Monitor: Output voltage versus time.

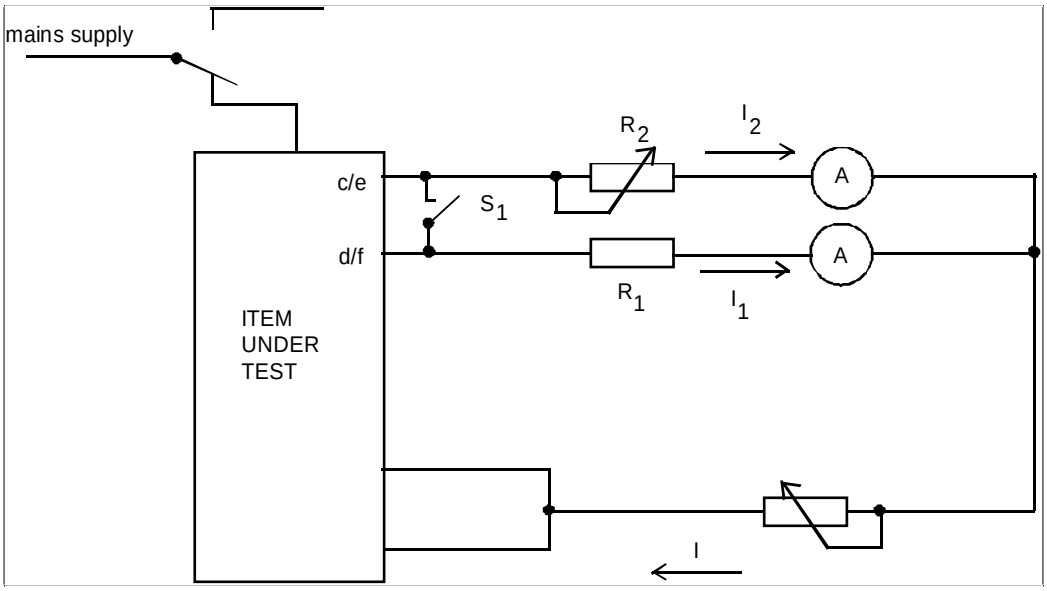
Results: The output voltage shall not drop below the minimum value of 34 V during the test.

E.5.1.8 DC unbalance of power source 1 (subclause 7.2.1.1, ETS 300 012)

NOTE: This requirement also applies to the APS.

Purpose: To test the DC unbalance of power source 1.

Test configuration:



R : adjust R for drawing max. power provided by PS1.
$R_1 = 2\ \Omega$

NOTE: Switch S1 is only used for calibration as follows : switch on, adjust R2 so that the same current is flowing in both wires, then switch off.

System State: Any state.

Stimulus: Drawing the maximum power provided by PS1 as declared by the apparatus supplier.

Monitor: Supply current in each wire.

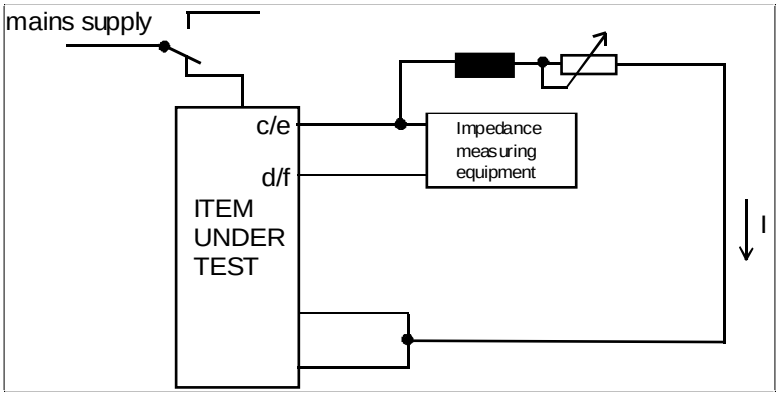
Results: The direct current unbalance X shall be less than 3 % of the current I *(I = I1 + I2)*, flowing through both phantom pairs.

$$x\ [\%] = \left| (I2 - I1) / (I2 + I1) \right| * 100$$

E.5.1.9 Current unbalance in a pair (subclause 7.2.2, ETS 300 012)

Purpose: To check influence of current unbalance to receiver and transmitter impedance.

Test configuration:



System State: Deactivated *(state G1)*.

Stimulus: Sinusoidal voltage of 100 mV rms, in the frequency range 2 kHz to 20 kHz. In addition, a direct current I of 3 % of the maximum current provided by the IUT is drawn, which should be adjusted by resistor R.

NOTE: It is not necessary to draw the maximum load current, since only the current difference of two wires of one pair can affect the impedance. The resistor R is high resistant, its influence can be neglected *(it is connected in parallel to the half of the coil of input or output transformer)*. In addition, a choke *(L)* can be connected in series to R.

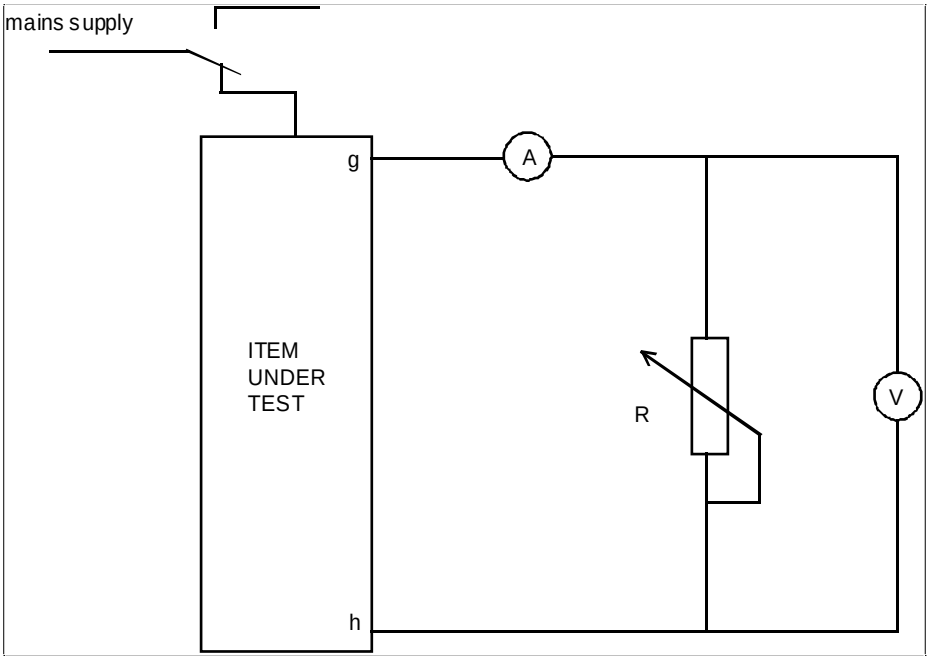
Monitor: Input/output impedance over frequency.

Results: The impedance of transmitter and receiver shall exceed the impedance indicated by template figure 11/I.430 [2].

E.5.2 Minimum voltage of power source 2 (subclause A.9.2.3, ETS 300 012)

Purpose: To measure the IUT voltage available at the access point.

Test configuration:



System state: Any state in normal and restricted modes.

Stimulus: Drawing no power and up to the maximum power provided by the IUT as declared by the apparatus supplier. Reduce the resistance from infinity ohms to a value, so that the maximum power is available according to the power mode.

Monitor: DC voltage and current.

Results: The voltage at the output of the source shall be 40 V *(+ 5/ -20 %)*.

E.6 Auxiliary power supply

E.6.1 Additional requirements from an APS (subclause 7.3, ETS 300 012)

There are three possible ways of powering a terminal connected to the ISDN passive bus configuration, one of which is phantom powering - deriving power from the differential voltage on the S interface. This method of powering is known in CCITT Recommendation I/430 [2] as power source PS1.

Power source 1 has the possibility of being in one of two states, normal powering and restricted powering. It is mandatory for the Network Termination *(NT)* to provide power source 1 in restricted powering mode. However, normal powering is optional, but can be achieved using the Auxiliary Power Supply, *(APS)*, i.e. 40 V + 5/- 15 % at the APS output.

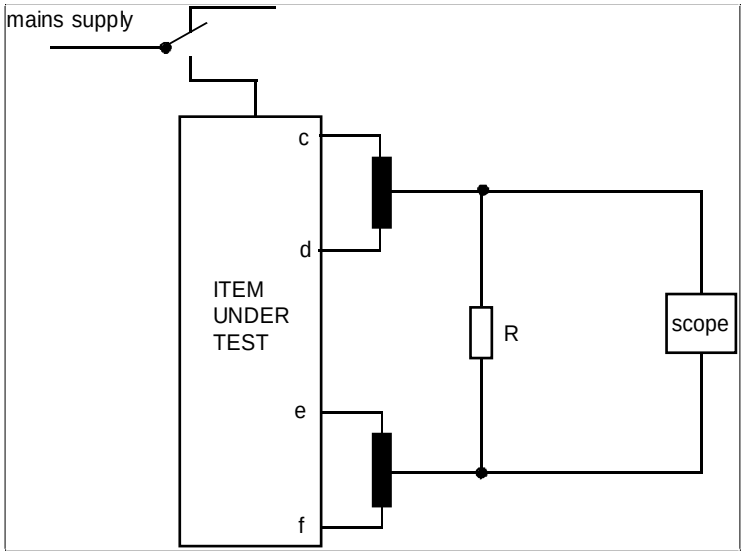
The APS is physically separate from the NT and can be connected at any point in the interface wiring. If an APS is located inside the same physical equipment as a TE and using the same plug, the power feeding requirements of the TE have to be taken into account. When the TE is a designated one, the APS power consumption when switched off cannot be measured. In this case, the power consumption shall be in accordance with the requirements for designated TEs.

Connection to the S interface wiring is via prEN 28 877 [4]. The APS shall continuously transmit INFO 0 and thus have impedance template similar to that of Terminal Equipment *(TE)* transmitting binary ONEs *(see figure 12-I.430 [2])*.

E.6.1.1 APS switch-on time (subclause 7.3.2, ETS 300 012)

Purpose: To ensure that the APS supplies a stable voltage of + 34 V within 2,5 ms.

Test configuration:



$R \approx (n + 1) * 1\ W$ at 40 V

System state: Any state and a test load R connected across the APS output.

Stimulus: APS is powered up in all possible sequences (according to the procedures in the supplier's declaration).

Monitor: Voltage with respect to time across the APS output.

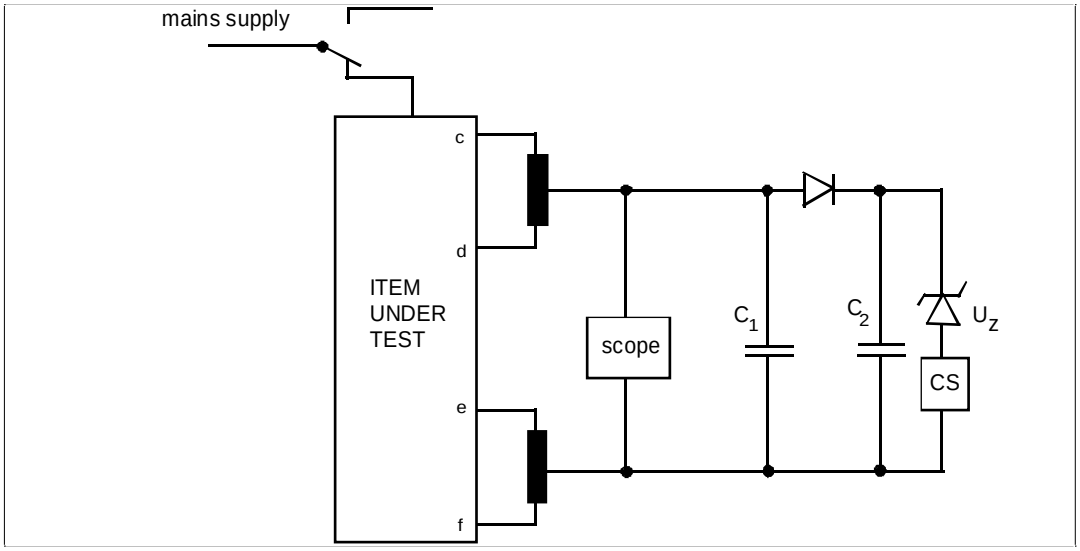
Results: The access lead pair c-d shall be positive with respect to the access lead pair e-f.

2,5 ms after the trigger point the voltage shall be ≥ 34 V, but ≤ 42 V and does not go below 34 V for a further period of at least 2,5 ms.

E.6.1.2 APS switch-off time (subclause 7.3.3, ETS 300 012)

Purpose: To ensure that the time taken for the normal output voltage from the APS to fall from + 34 V to + 1 V is within 2,5 ms.

Test configuration :



CS = 15 mA U_z = 15 V C_1 = 100 nF C_2 = 100 µF

System state: Any state and a test load connected to the transmit and receive pairs.

Stimulus: The input power to the APS is removed in all possible sequences *(according to the procedures in the supplier's declaration)*.

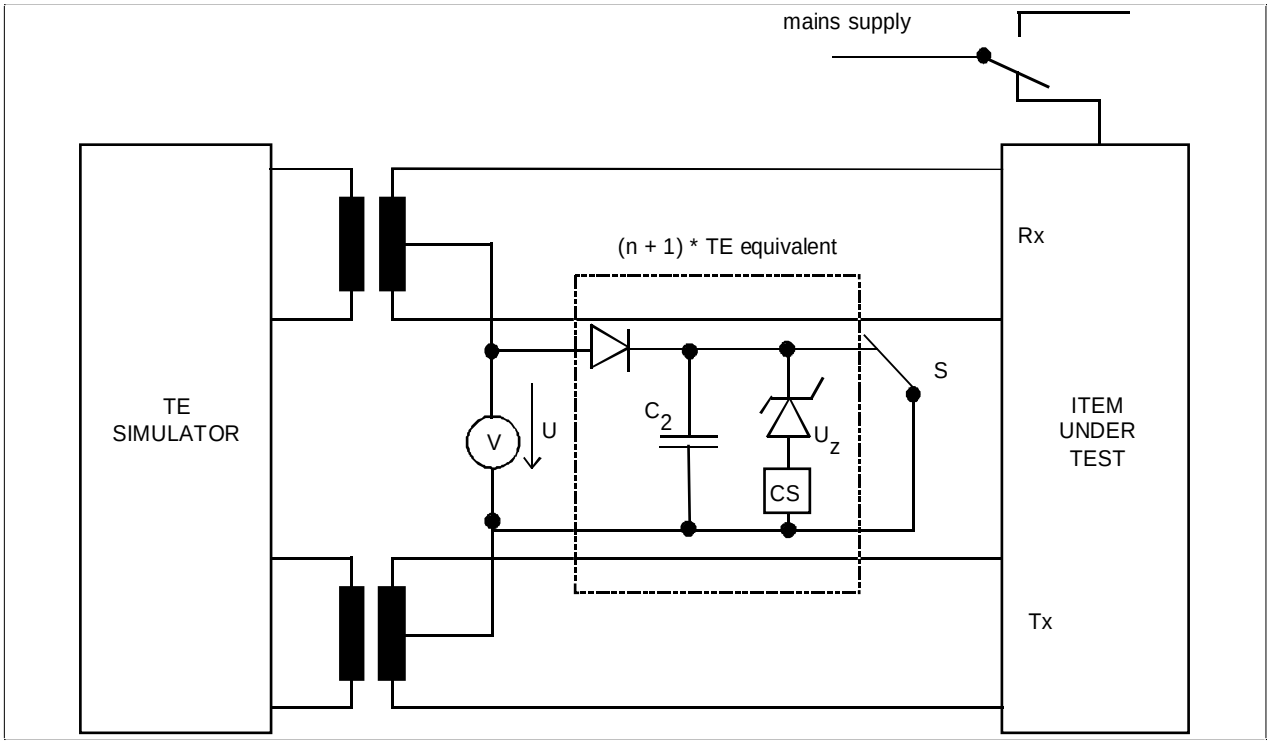
Monitor: Voltage with respect to time across the APS output.

Results: 2,5 ms after the trigger point the voltage shall be ≤ 1 V and does not rise above 1 V for a further period of at least 2,5 ms.

E.6.1.3 APS requirements for type "a" sources (subclause 7.1.4.3, ETS 300 012)

Purpose: To test requirements for voltage increase of an APS, with fall-back characteristics, after removal of a short circuit.

Test configuration :



System State: Any state.

Stimulus: Lowest acceptable voltage level at mains interface, short-circuit steady state of 30 minutes, removal of short-circuit *(switch-off : S)*, with a load of n + 1 TE-equivalents as given in figure 4 of ETS 300 012.

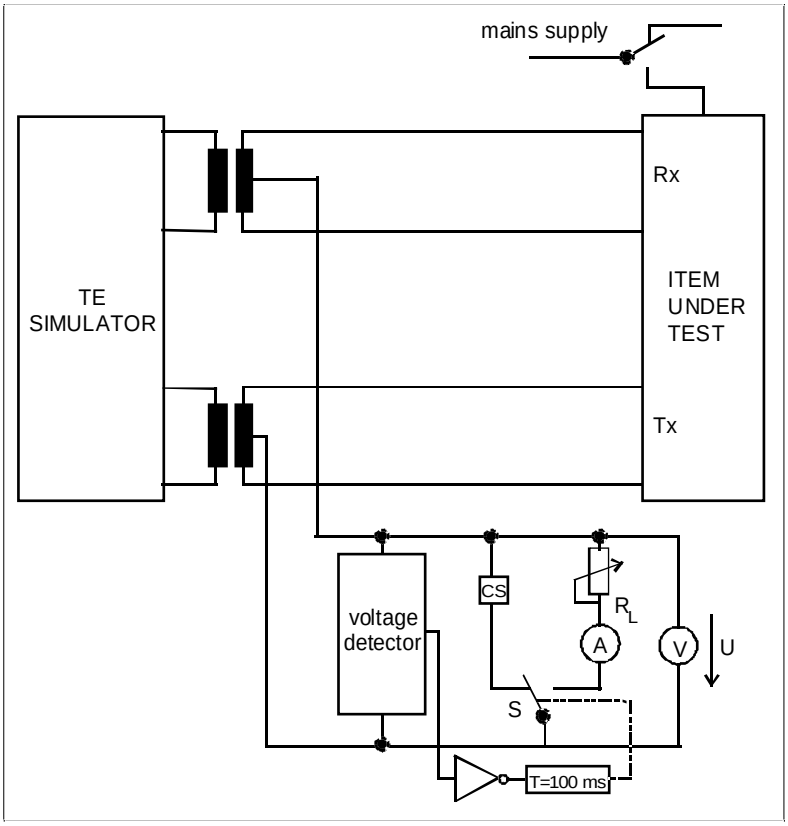
Monitor: Output voltage under n + 1 times TE-equivalents.

Results: Output voltage shall increase from 1,0 V to 34 V within 350 msec. This shall appear within 10 seconds after the removal of the short circuit.

E.6.1.4 APS switch on surge capability (subclause 7.1.4.4.1, ETS 300 012)

Purpose: Switch-on surge capability, APS in normal mode.

Test configuration:



System State: Any state.

Stimulus: Connection of mains supply.

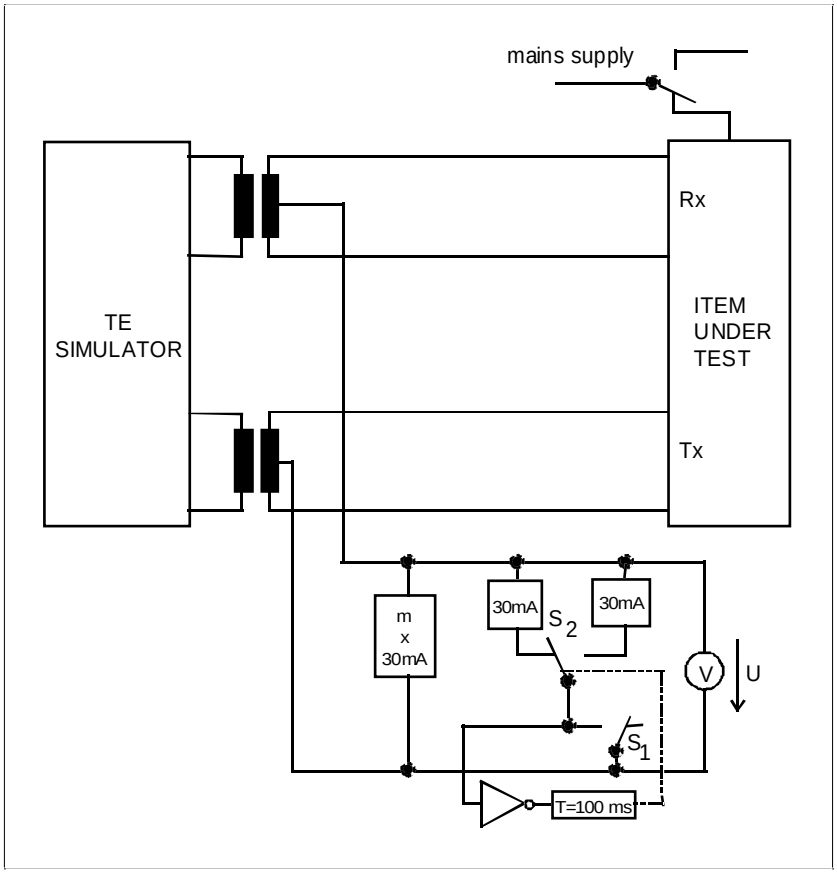
Monitor: Output voltage versus time.

Results: The power source 1 shall provide a minimum current of n+1 times 45 mA for at least 100 ms and the voltage shall be at least 30 V during this time period.
After the time of 100 ms, the power source shall be able to provide the power of n + 1 times 1 Watt and the drop of power on the interface with the output voltage shall be within the specified limits.

E.6.1.5 APS TE connection surge capability (subclause 7.1.4.4.2, ETS 300 012)

Purpose: TE connection surge capability in normal mode.

Test configuration:



System State: Any state.

Stimulus: Switch on S_1 and then after a delay of 100 ms switch-on S_2.

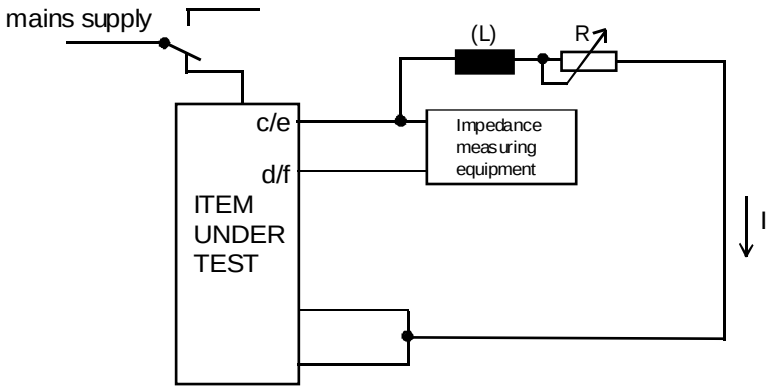
Monitor: Output voltage versus time.

Results: The output voltage shall not drop below the minimum value of 34 V during the test.

E.6.1.6 APS current unbalance in a pair (subclause 7.2.2, ETS 300 012)

Purpose: To check influence of current unbalance to receiver and transmitter impedance.

Test configuration:



System State: Deactivated *(state G1)*.

Stimulus: Sinusoidal voltage of 100 mV rms, in the frequency range 2 kHz to 20 kHz. In addition, a direct current I of 3 % of the maximum current provided by the IUT is drawn, which should be adjusted by resistor R.

NOTE: It is not necessary to draw the maximum load current, since only the current difference of two wires of one pair can affect the impedance. The resistor R is high resistant, its influence can be neglected *(it is connected in parallel to the half of the coil of input or output transformer)*. In addition, a choke *(L)* can be connected in series to R.

Monitor: Input/output impedance over frequency.

Results: The impedance of transmitter and receiver shall exceed the impedance indicated by template figure 12/I.430 [2].

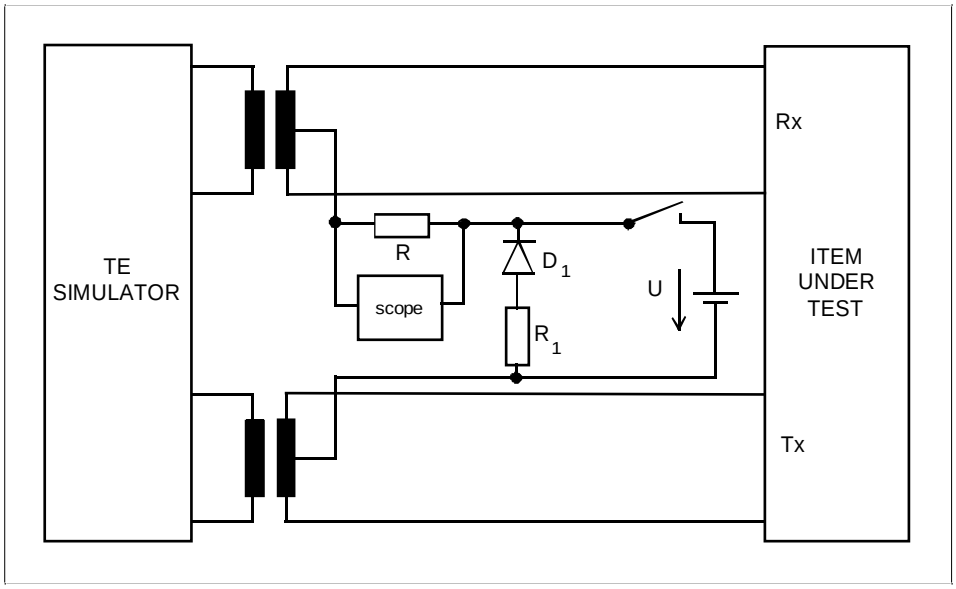
E.6.2 Additional requirements for NT compatible with APS (subclause 7.4, ETS 300 012)

The NT designed to be compatible with an APS shall not have a PS1 normal mode source. However, the NT shall have the capability of supplying PS1 restricted mode source.

E.6.2.1 Power source 1 mode back-off (subclause 7.4.1, ETS 300 012)

Purpose: To ensure that the NT can switch-off the restricted mode power source on detection of PS1 normal mode on the passive bus.

Test configuration:



$(R + R_1 + D_1) \approx 420$ mW

System state: Any state.

Stimulus: NT supplying PS1 restricted mode to the passive bus.

Phantom supply voltage.

U = 40 V

R = 15 ohms

Monitor: Voltage with respect to time across the NT output.

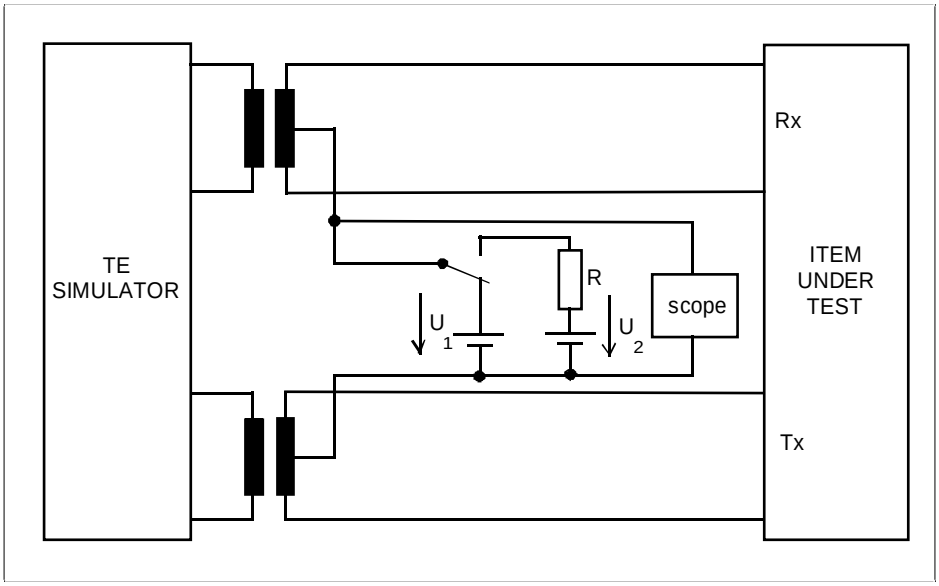
Results: The current or power drawn by the PS1 restricted shall be :

no limitation	for	$0\ s \leq t \leq 5\ \mu s$
≤ 45 mA	for	$5\ \mu s < t \leq 100$ ms
≤ 3 mW	for	$t > 100$ ms

E.6.2.2 Power source 1 restricted mode power-up (subclause 7.4.2, ETS 300 012)

Purpose: To ensure that the NT can switch to restricted mode power source on detection of a normal mode voltage between 2 V and 5 V *(loss of PS1 normal mode).*

Test configuration:



U_1 = 24 V R = 3.8 kΩ ≈ 420 mW at 40 V

System state: Any state.

Stimulus: Switch-over from U_1 to U_2.
a) U_2 = 5 V
b) U_2 = 2 V

Monitor: The phantom voltage of the NT.

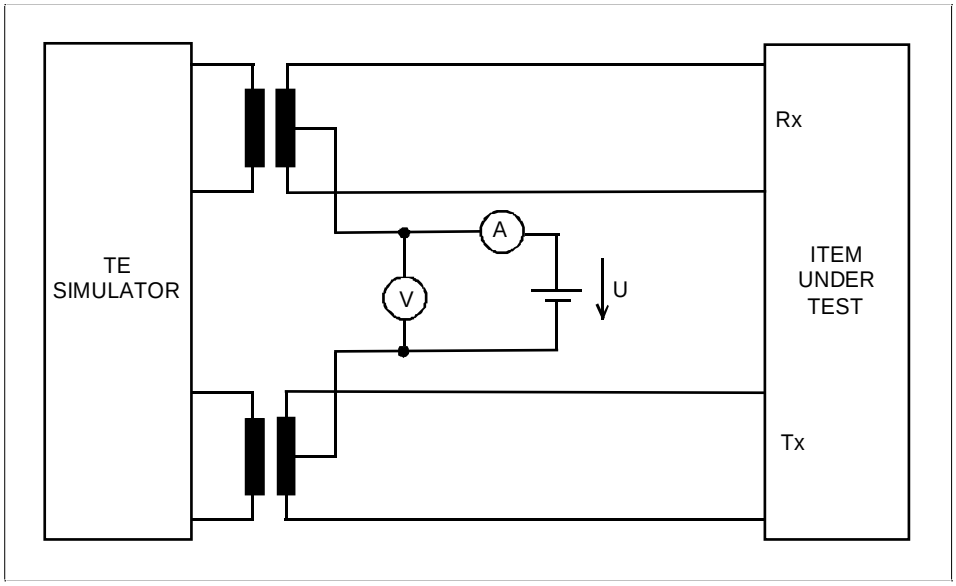
Results:
a) the voltage shall be equal to 5 V.

b) the NT shall drive the phantom voltage to rise - 34 V *(but not exceeding - 42 V)* within 2,5 ms after the switch-over from U_1 to U_2. For a further 2,5 ms the phantom voltage shall be in the range from - 34 V to 42 V.

E.6.2.3 Power consumption from APS normal mode (subclause 7.4.3, ETS 300 012)

Purpose: To ensure that the NT does not consume more than 3 mW from the passive bus when the APS is supplying PS1 normal mode.

Test configuration:



System state: Any state.

Stimulus: Phantom normal mode Power Source 1 in the voltage range 40 V, + 5 % / - 40 % *(42 V to 24 V)*.

Monitor: DC voltage and current in the access leads.

Results: The power consumed by the NT shall not exceed 3 mW at both extremes of the power source voltage as stated in the stimulus section. This does not apply for the first 100 ms after the connection of the power source.

History

Document history	
April 1992	First Edition
January 1996	Converted into Adobe Acrobat Portable Document Format (PDF)